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ANALYSIS OF 6T SRAM CELL USING FINFET AT NANOMETER REGIME

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ABSTRACT
The fast growing technology developments in the metal oxide semiconductor area have scaled down CMOS to the sub 32nm regime. According to International Technology Roadmap For Semiconductors projection by the 2020, the printed gate lengths will scale down to 12nm. Instead of SiO2 with AL metal gate Hafnium Oxide [HFO2] can be used as a High k material. To increased chip functionality demand, SRAM area have mostly exceed overall chip area. The stability of SRAM cell depends on variation in Process, Temperature and Voltage. This paper will discuss the detail about 6T SRAM stability in standby, read and write mode design considering Double Gate MOSFET at 32nm technology node.

KEYWORDS: Cell Ratio (CR), Pull up Ratio(PR), Silicon on Insulator(SOI), Static Random Access Memory(SRAM), Static Noise Margin.

INTRODUCTION

Static Random Access Memories are used in various microelectronics applications such as wireless, system on chip, multimedia applications, server processor etc. By using transistor scaling i.e. size reduction has increased the performance with decreasing the cost of integrated circuit. In integrated systems, SRAM cell are used for high integration density with the required performance and reliability. SRAM cell are used for increasing storage density, reducing supply voltage i.e. VDD for standby power consumption. Also used for multiple SRAM arrays and reducing size of transistor.
Decreasing the device dimension limits the performance of MOSFET due to presence of impurity, increase in gate tunneling effect and also increasing p-n junction leakage current. There are two issues while designing SRAM cell: The cell area and its stability. The overall chip density can be determines by using its cell area. Whereas the operating conditions, sensitivity of the memory to process tolerance and the soft error rate determines the cell stability.
J. Lohstroh, K.Anami and F.J.Listhave analyzed that the stability of SRAM cell can be expressed by using static noise margin. Later on in 1987 E.Sevinch found the static noise margin of SRAM cells by using analytically as well as simulated result. In 2006, Evelyn Grossar proved stability of N curve for finding stability of read and write. In 2008, Zheng derived various methods for calculating the read and write stability. Jiajing Wang, Satyanand Nalam, and Benton H. Calhoun, analyzed various parameters affecting the performance of SRAM such as power consumption, static noise margin, effect of process, temperature and power supply. Benton H. Calhoun proved that transistor scaling and word line voltage modulation affects the stability.

6T SRAM WORKING AND FAILURE MECHANISM :

The given figure shows the basic six transistor cell formed for CMOS static random access memories. It also consist of two cross coupled CMOS inverters for storing one bit information. The two n type transistor i.e. M2 and M5 are known as access transistor which are connected to word line i.e. WL for accessing read and write operation through bit lines BL and BLB.

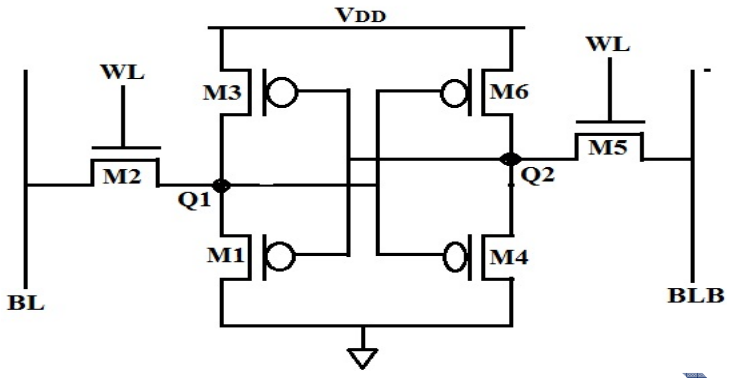

Figure 1: Basic 6T SRAM Cell

6T SRAM WORKING

Basically SRAM cell operates in Read, Write and Standby mode. In read mode the bit lines are pre charged to high level i.e. VDD and word line is selected by pulsing to the high level. At the cell storing side a logical low voltage i.e. '0', the bit line is discharged through the access pull down and access transistor for developing differential voltage across bit lines. For detecting the state of the cell, differential voltage should be high for sensing amplifier. Also differential voltage should not be too high to avoid the cross coupled inverters to flip in their state. For reducing the read disturbance, the cell ratio i.e. aspect ratio of the access transistor and pull down transistor should be large.

In write mode the bit lines are access in complementary voltage levels through a write driver and word line is selected. At the cell storing side the bit line voltage is logical low i.e. '0' and through the access transistor, the internal storage nodes are discharged. By using cross coupled inverters the voltage gets raised on the opposite storage node. In short the restoring strength of the pullup transistor should be less than discharging strength of the access transistor. The ratio of pullup transistor to the strength of the pass gate transistor should be high to avoid write failure.

Whereas in standby mode, the cell stores the data indefinitely till it is connected to VDD. So in standby mode the word line is grounded.

FAILURE MECHANISMS :-

We should take care of various SRAM cell parameters while designing SRAM to avoid failure due to read, write and hold case.

READ FAILURE :

Failure occurs while reading content of SRAM cell is known as a read failure. Consider that node X storing a logical low i.e. '0' and bit lines is discharging through M1 and M2. If the width of access transistor M2 is less than that of pull down transistor M1. Therefore, resistive divider is formed by using M1 and M2 which develops a voltage ripple. The cell state starts flip while reading only when a voltage ripple is greater than the switching threshold of the given inverter formed by M4 and M6. By rising the difference between the trip point of inverter related with the node storing logical high i.e. '1' and the voltage rise at the node storing logical low i.e. '0' can reduce the read failure in SRAM.

WRITE FAILURE :

If the node storing logical high is unable to discharge through the access transistor during the word line turn on time causes write failure to the SRAM cell. By increasing the write access time with word line turn on time can reduce the write failure. But SRAM gets slower while increasing word line turn with write access.

ACCESS FAILURE :

If the voltage difference between the two bit lines at the time of firing sense amplifier is below the threshold voltage of the given sense amplifier causes access failure. This is caused due to the reduction of the bit line discharging current across the pull down resister and the pass transistor. Creating the stronger pull down transistor by decreasing the resistance in the discharge path can make a faster bit line discharge.

HOLD FAILURE :

A high leakage occurs at the pull down NMOS transistors connected to the node storing logical high causes hold failure. If the voltage at lower VDD is less than the trip point of the inverter storing logical low causes the cell flips in the hold mode. The hold failure can be minimized by reducing the leakage in the standby mode using high VT pull down transistor.

CONCLUSION

This paper analyzed various methods for finding the stability while designing 6T SRAM cell in read, write and standby mode. While designing various failure mechanisms such as read, write access and hold failure. Also various factors are consider such as power supply, cell ratio, bit lines, word line voltage and threshold voltage. The stability of SRAM in read mode increases with cell ratio whereas the pull up ratio affects only write mode. That means stability in write mode increases with decrease in pull up ratio. Also increase temperature decreases the stability of SRAM in read and standby mode.

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