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DESIGN LBIST USING STUMPS ARCHITECTURE

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Abstract
The rapidly increasing complexity of IC designs makes testing of VLSI chips more difficult due to occurrence of faults in the VLSI chips. This lead to development of testing technology called Logic Built in Self-Test (L-BIST). Design of reconfigurable Linear Feedback Shift Register (LFSR) for VLSI IC testing is implemented in LBIST. Reconfigurable LFSR can be used in logic BIST for improvement in Fault coverage of IC testing. Self-Test Using MISR/Parallel SRSG (STUMPS) architecture is used in logic BIST. The main intention of this paper work is to understand the performance and design of LBIST using STUMPS for VLSI IC testing and analyzing speed, fault coverage and power.

Keywords: BIST, LBIST, LFSR, MISR, STUMPS

1. Introduction

In modern era, with ever-increasing chip density, make IC designs more complex and difficult for testing of VLSI chips. Advancement in manufacturing technologies makes VLSI chips more difficult for test due to occurrence of faults. Built-in self-test (BIST) has become one of the preferred test technologies. BIST strategy allows rapid testing of the circuit. The Linear feedback shift registers (LFSR's) is used to generate pseudorandom patterns in the BIST due to its low hardware costs.

The basic idea of BIST is to design a circuit so that the circuit can self-test and determine either it is good or bad (fault-free or faulty). This requires functionality of self-testing feature and the additional circuitry. This additional circuitry must be capable of generating test patterns and provide a mechanism to determine output responses of the circuit under test (CUT) is faulty or fault-free.

Typical LBIST consists of test pattern generator, circuit under test, LFSR, multiple input shift register (MISR) and BIST controller. The Pseudo Random Pattern Generator (PRPG) is implemented using an LFSR which generates random test patterns. LFSR structure includes XOR gates, flip-flops and multiplexers that make it reconfigurable.

LFSR has a characteristic polynomial that gives details of its behaviour. Coefficient of characteristic polynomials is 0 or 1 as it shows presence or absence of the tab position in LFSR. Characteristics polynomial produces patterns which are pseudorandom patterns and having maximum length, patterns repeat only after producing the maximum number of possible patterns.

LBIST architecture PRPG act as the test pattern generator and these test patterns are inputs to the circuit under test. Outputs from MISR is compared with the expected outputs (Golden signature) using a comparator to check whether the circuit under test is fault-free or faulty.

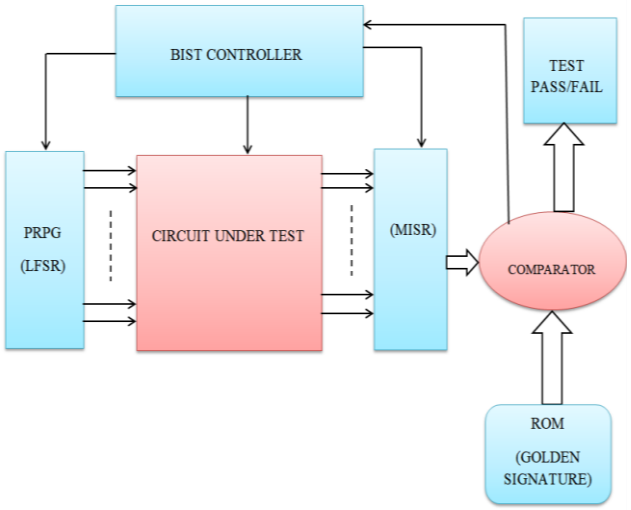

Fig.1 General Block diagram of logic BIST [4]

The BIST controller is the important part of the BIST system which coordinates with different blocks of BIST for proper operations of the different blocks. Based on the test mode input to the BIST controller, the system either operates in the test mode or in the normal mode. [3]

Benefits of BIST are it significantly reduces cost of automatic test pattern generation. It reduces storage and maintenance of test patterns. It can test many units in parallel. It takes shorter test application times

2. Proposed Design

The LBIST with STUMPS (Self-Test Using a MISR and Parallel Shift register sequence generator) architecture using reconfigurable LFSR is consider for VLSI IC testing purpose. STUMPS architecture significantly reduces test

time of scan BIST approaches by taking benefits of multiple scan chains.

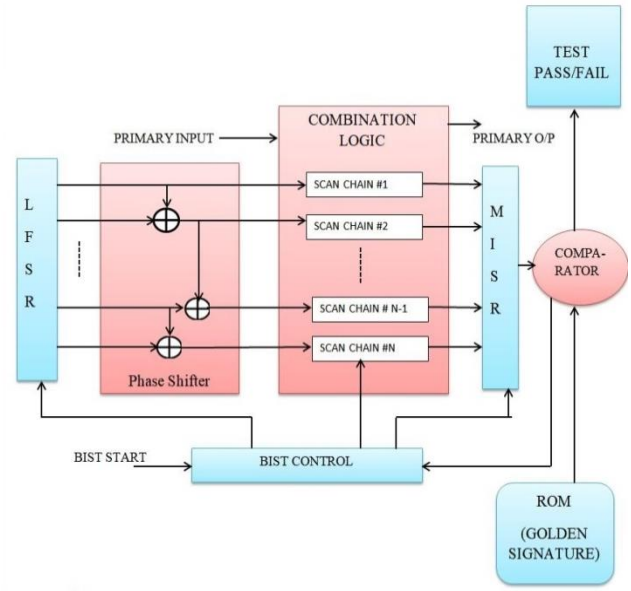

Fig.2 LBIST scan with phase shifter [6]

MISR is used to reduce the amount of hardware necessary to compress a multiple bit stream. Standard and hybrid are the type of LFSR which are implements in logic BIST architecture. BIST controller is the most important part of the BIST system. BIST controller that we want to designed must follows the STUMPS architecture. Based on the test mode input of controller, the system operates in the normal mode or in the test mode (TM).

When the TM is 1, system enters into test mode, it gives enable signal to the LFSR then it generates the patterns which are given as inputs to the CUT and then it gives signal to MISR for the compression of patterns from the CUT.

Phase shifter is used to avoid structural problem which arise in multiple scan. Phase shifters manipulate multiple bits in parallel as they leave the LFSR or register and enter the scan chains. Phase shifter is composed of exclusive-OR gates. Phase shifter is essential for proper working of the system.

Standard and hybrid LFSR is comparing with respect to power, speed, and frequency. The fault coverage can also calculate. Xilinx ISE software is used for synthesis the system design.

2.1 LFSR Types

The LFSR generally used for implementations in BIST applications because LFSR is more area efficient than a counter and it also require less combinational logic per flip-flop. LFSR have following types which we consider for designing the system architecture and we compare them.

2.1.1 Standard LFSR

Standard LFSR is a shift register XOR gates that represent tap positions of feedback polynomials and which are properly interconnected to produce a new output bit.

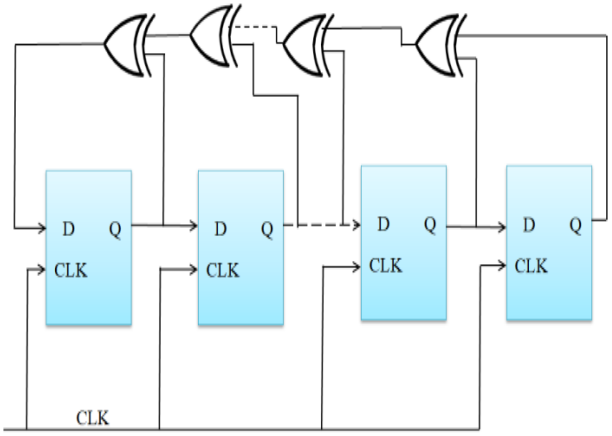

Fig.3 Standard LFSR [4]

2.1.2 Hybrid LFSR

Benefits of Hybrid structure of LFSR compared to standard form is that the number of XOR gates required can be reduced from ‘n’ XOR gates to the (n -1)/2 in hybrid form.

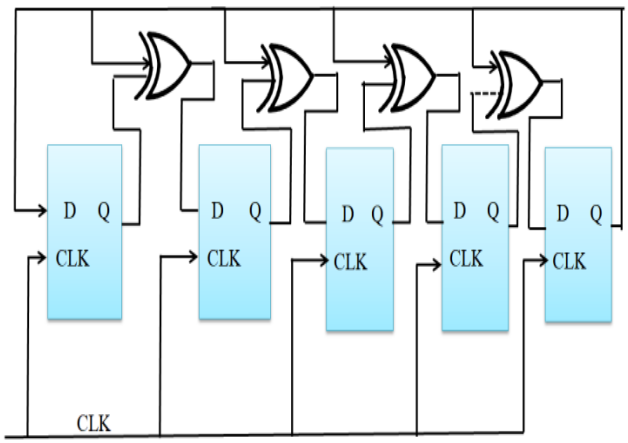

Fig.4 Hybrid LFSR [4]

Hybrid LFSR is more efficient in terms of number of gates, area and speed.

2.2 MISR

A MISR is used to minimize the amount of hardware required to compress a multiple bit stream. The MISR provides a replacement for using multiple LFSRs in parallel and separately comparing the error polynomials.

2.3 Golden Signature

Signature refers to any statistical property which is capable of differentiating between good and bad circuits. Golden signature refers to the good machine signature which is the output response of the MISR when the circuit is working perfectly.

2.4 Circuit under Test

The circuit that is to be tested is called as the circuit Under Test or the CUT. It is the circuit of the IC that is checked for any faults after its manufacturing for the result. The input to the CUT is driven by LFSR and CUT output is given to MISR and it also coordinate with BIST controller in order to provide result.

2.5 BIST Controller

BIST controller that we want to designed must follows the STUMPS architecture and it also coordinate with different block in LBIST such as LFSR, MISR, and combinational logic block. The controller work according to input test mode signal, if test mode is given as 1 then test mode is activated else it work in normal mode.

2.6 Phase Shifter

Phase shifter is made up of exclusive-OR gates. Phase shifter is used to avoid structural problem which arise in multiple scan.

2.7 Seeding

Seed will be given for different size and the LFSR generate patterns corresponding to that size and seed. For each different seed it produces different patterns. Seeding plays a vital role for patterns to be generated. It can be done by various methods one of the method is gauss elimination seeding method.

2.8 Primitive Polynomials

Polynomials which give result in the form of maximum length sequence are called primitive polynomials. Primitive polynomials produce a maximum length sequence without considering implementation is of the internal or external feedback type.

2.9 Operational Overview

The BIST controller gives input to LFSR and enables it. LFSR with PRPG generates pseudorandom patterns and it fed to CUT. CUT is checked using STUMPS architecture, when input is given to CUT the scan chain work and generates output which is given to MISR for reducing size. If circuit is faulty then pattern generated by CUT according to LFSR output response will be different from expected output from golden signature and hence we get the final result.

3. Result

The work done previously reported the following results: The fault coverage is calculated for different circuit for different time, time analysis was performed as well as the different performance parameter is checked.

Performance parameter	Standard LFSR	Hybrid LFSR
Number of Flip-flop	32	32
Number of 4 input LUT	33	33
Maximum frequency of operation	368.684	378.652

Table 1 Parametric analysis for different 32 bit LFSR in XILINX SPARTAN 3E FPGA [4]

Quantity		Value
Minimum period	BIST with LFSR	4.088 ns

Table 2 Timing analysis [3]

The above expected result should be obtained by our proposed system with better results.

4. Conclusion

The LBIST with reconfigurable LFSR using STUMPS architecture compare standard and hybrid types of LFSR and test various parameters of VLSI chips. Fault coverage, speed, time and power parameter also take in consideration. As future scope the advancement in low power reconfigurable LFSR can be developed as well as power can reduced using power gating technique.

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