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DESIGN OF BAND GAP REFERENCE CIRCUIT FOR SUB 1-V OPERATION WITH LOW SUPPLY VOLTAGE

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Abstract

In design of an analog VLSI circuits it is important to create current and voltage reference circuits. These reference circuits are expected to produce constant output voltages against various supply voltages, process parameters and temperature variations. This Band Gap Reference (BGR) is proposed to successfully operate at sub-1V with supply voltage of 1.2V with expected reference voltage of 600mV. The main intention of this paper work is to explore the performance and design of BGR. It should provide stable dc output voltage in all process corners. In this paper detailed designof OP-AMP is also given. BGR circuit which is capable of producing constant output voltage for given supply voltage is implemented in 45nm CMOS technology. The testing of MOSFET device for process corners is presented.

Keywords: Analog, BGR, CMOS, MOSFET, OP-AMP, VLSI

1. Introduction

Bandgap voltage references are critical building blocks for variety of analog and mixed signal circuit applications in VLSI. BGR circuit provides stable DC reference voltage which is robust against process, voltage and temperature variations due to various conditions. Reference voltage generator circuits are widely used in analog to digital convertors, regulators, DRAM etc where constant reference voltage is needed. In such circuits reference voltage accuracy plays important role in determining performance of circuit. BGR has very less dependency on temperature and power supply.

SUB-1V reference generation has got much importance due to scaling resulting in reduction of MOS transistor dimensions and also reduction in power supply. In present era a demand for small size and low power circuits is increasing gradually. As a result automatically demand for small size and SUB-1V BGR circuit is also increasing. For size of BGR number of diodes is critical factor, because diodes are made from bipolar junction transistors (BJT). Generally size of BJTs is very large as compared to MOS transistors. Thus the number of transistors must be reduced to reduce overall active area.

Reference voltage may vary with temperature. Voltage reference circuit is very much precise at its output signal, provide stability and consume less power. Therefore reference voltage performance can be evaluated by its reliability and accuracy. The operation principle of BGR circuit is based on generation of two voltages (PTAT & CTAT) which are opposite to each other. PTAT is proportional to absolute temperature which increases with increase in temperature. CTAT is complimentary to absolute temperature which decreases with increase in temperature. The stability of output reference voltage is obtained by adding these two voltages, which compensate the changes in temperature.

The generator circuits are required to be stabilized over process, voltage and temperature variations and also to be implemented without any modification in fabrication process. The BGR is one of the most popular reference voltage generators which achieve the required specifications. The demand for low power and low voltage operation is strongly increasing in battery operated portable devices.

One of the most used topology for designing BGR is with use of operational amplifier, few resistors and several BJTs. BGR performance depend strongly on performance of amplifier used. The design uses linear combination of BJT which is limited by non linear dependence of base emitter voltage.

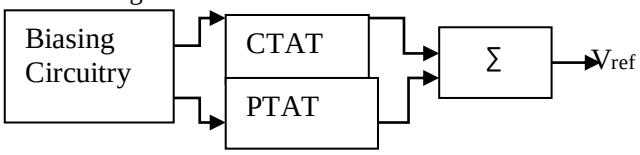

Fig. 1. Block diagram of BGR

There are many alternatives to understand and realize voltage references in VLSI Integrated Circuits. In this paper proposed approach is cancelling the CTAT dependence from BJTs which are pn junction diodes with positive temperature dependence from PTAT circuit which uses several resistors and transistors. BGR proposed in this paper provides a steady dc reference voltage in various operating conditions. The output reference voltage produced by BGR should be insensitive to power supply, process corners and also to the temperature variations. BGR should provide constant output reference voltage for different fabrication process. The BGR presented in this paper has low output reference voltage with voltage supply of 1.2 V.

2. Proposed BGR Circuit

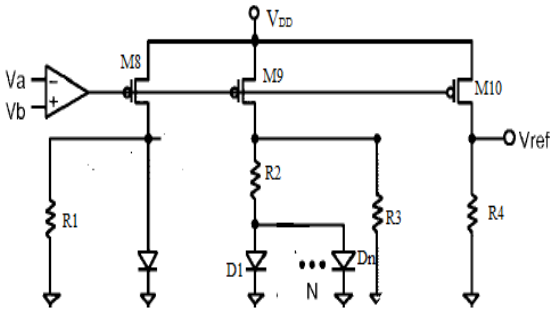

Fig. 2. Proposed BGR Circuit for SUB 1-V

The BGR circuit which produces reference voltage definitely below 1 Vhas been proposed in Fig. 2. This circuit consists of several BJTs which will act as pn junction diodes, few resistors and transistors. CTAT current can be calculated from Q1. PTAT current can be calculated from resistor R1 and number of diodes parallel in second branch.

$$I_{PTAT} = \frac{V_T ln(n) R_3}{R_2} \quad (1)$$

Here V_T is thermal voltage,

n is the number of diodes parallel in second branch

$$V_T = \frac{KT}{q} (2)$$

K is the Boltzmann Constant and q is the electronic charge.

$$I_{CTAT} = \frac{V_{BE}}{R_1} \quad (3)$$

In this circuit, from above equations it is clear that branch one will produce CTAT current and branch two will produce PTAT current.

The output reference voltage of BGR can be calculated by simply adding the PTAT and CTAT voltages. These voltages are added in such way that they can cancel outTemperature Coefficient(TC) effect and produce stable reference voltage which has zero Temperature Coefficient effect. While designing this BGR circuit it is necessary that branch one and branch two get equal amount of current. For that purpose two stage OP-AMP is used in the circuit. OP-AMP provides steady power supply to both PTAT and CTAT branches. Here two stage OP-AMP is used.

$$V_{ref} = R_4 \left[\frac{V_{BE}}{R_1} + \frac{R_3 V_T ln(n)}{R_2} \right] \quad (4)$$

2.1.Two Stage OP-AMP Circuit

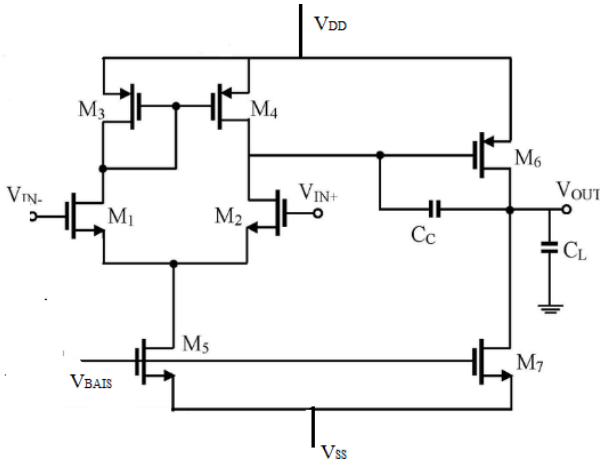

Fig. 3. Two stage OP-AMP

Fig. 3 shows circuit diagram of two stage OP-AMP. This OP-AMP consists of two stages. First stage is differential amplifier followed by second stage consist of a current source amplifier. Two stage OP-AMP is used because of its high precision at stability. Two stage OP-AMP provides sufficient gain. Differential amplifier consists of transistor M1-M5. Both the inputs of amplifier are of same potential.

The proposed circuit consists of two stages so the one extra pole is come into the circuit. This pole may lead to improper circuit operation which cause sudden falls in phase response. So for proper circuit operation we need good phase margin so there is fast settling and ringing is less. For that purpose miller compensation technique is used. The capacitor Cc is miller capacitance.

Aspect ratio of various transistors is calculated by considering various factors. Current through OP-amp is

calculated from slew rate. Size of transistors M1 and M2 is calculated from GBW. Similarly size of transistors M3, M4 and M5 is calculated from ICMR. Gain of an amplifier is decides such way that there will be less ringing in BGR circuit and settling time will be fast.

2.1.1 Design Calculations:

$\left(\frac{W}{L}\right)1,2$, I_0, $\left(\frac{W}{L}\right)3,4$ *and* $\left(\frac{W}{L}\right)5$ are calculated from equations (5) to (8).

$$GBW = \frac{g_m}{C_L} \quad (5)$$

$$SR = \frac{I_0}{C_L} \quad (6)$$

$$V_{in(min)} = ICMR(-) \quad (7)$$

$$V_{in(max)} = ICMR(+) \quad (8)$$

3. Results

PMOS and NMOS transistors are simulated to study effect of process corner and temperature variations on current through device. The effects on drain current are within limit and acceptable in BGR. Table 1 shows these values with respect to temperature variations.

Table 1. Simulation result table

	PMOS				NMOS	
	-40	27	125	-40	27	125
TT	26.63 uA	22.59 uA	17.82 uA	27.85 uA	22.19 uA	16.7 uA
FF	39.18 uA	32.44 uA	24.26 uA	45.40 uA	35.02 uA	25.20 uA
SS	15.80 uA	14.25 uA	12.04 uA	13.22 uA	11.45 uA	09.40 uA

Drain current of MOSFET varies with change in process corners and temperatures. It is minimum at slow corner and maximum at fast corner.

4. Conclusion

CMOS BGR circuit which can generate reference voltage below 1 V has been proposed. BGR produces reference voltage by adding PTAT and CTAT voltages. Two stage OP-AMP circuit is also proposed here. Effect of process corner and temperature variations on drain current of transistor is also verified.

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References

[1] S. Mehrmanesh, M. B. Vahidfar" A 1 Volt, High PSRR, CMOS Band Gap Reference," *IEEE*, 381-384. Mar 2003.

[2] Jonathan P, Nuno Horta, " Design of a BGR Suitable for The Space Industry with Performance of 1.25 V," *IEEE NGCAS*, 197-200. 2017.

[3] Anne Johan, Annema and Bram Nauta, "Analog Ciruits in Ultra-Deep Sub Micron CMOS," *IEEE Journal of Solid Statte Circuits*, 40(1), 132. 2005.

[4] Bonnie baker and Miro Oljaca, "How the voltage reference affects ADC Performance," Analog Applications Journal, Fourth Quarter, Texas Instruments, 9. 2009.

[5] Weng , Hsu, " A 1.8V high precision compensated CMOS bandgap reference," *IEEE Conference on Electronic Devices and Solid State Circuits*, 271. 2005.

[6] Charalambos M. Andreou, SavvasKoudounas, " A Novel Wide Temperature Range CMOS Bandgap Reference Circuit," *IEEE Journal of solid state circuits* , 47(2), 574. Feb 2012.

[7] Sanjay K Wadhwa, "A Low Voltage CMOS Bandgap Reference Circuit," *IEEE International Symposium on Circuits and Systems*, 2008.

[8] Pierazzi, Andrea et al, "Bandgap Reference for near 1-V Operation in Standard CMOS Technology," *IEEE Custom Integrated Systems Conference*, 463-466. 2001.

[9] C. W. Kok and W.S. Tam, " CMOS Voltage Reference:An Analytical and Practical Prespective," *IEEE Press*, 2013.

[10] Philip E. Allen and Dougles R. Holberg, " CMOS Analog Circuits Design," Third edition, Oxford University Press,2012.