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AN EFFICIENT IMPLEMENTATION OF POLAR ENCODER

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ABSTRACT
Proposed for promising high speed 5G system using radix 2r based polar encoder in VLSI architecture, including single radix and reconfigurable multi-radix modes. The polar codes are considered as one of the most favourable error correcting code because of its channel achieving property. This property helps to handle the long length codes. When code length is small, fully parallel encoder implementation is easy. But when the code length increases, the hardware implementation becomes more complex. To overcome the disadvantage of fully parallel encoder, partially parallel encoder is designed. The newly designed encoder handles long polar codes with less hardware complexity. The main advantage of proposed encoder architecture is less hardware complexity, reduced delay and detection of error and power consumption. Partially encoder architecture is designed and synthesized by using Xilinx 12.2. The results are simulated by using ModelSim 10.4a simulating tool.

INDEX TERMS-Polar codes, Polar encoder, Very-Large-Scale-Integration

I.INTRODUCTION

Polar codes are one of the appreciative error correcting due to its channel achieving property. It is now considered as the major enhancement in coding theory and it is used in data storage device application. Polar codes are now used in the 5^{th} generation wireless system(5g) formalization process of 3^{rd} generation partnership project (3GPP).This system has chosen the polar codes as a channel coding scheme .It is linear block error correcting code which is found in low computing complexity channels. The designing method for polar codes are channel combining and splitting. The best qualified error correcting code for the code having long length is the polar codes .The message in the storage system are safeguarded by the error correctingcodes. In 1948, the research on channel codes has developed for the past sixty years. The two codes have been newly discovered that approaches the Shannon limit are turbo codes and LDPC codes these two codes are used in communication and storage system due to their excellence in error-correcting capability. As these two codes were already successful in practical application, the search for furthermost capacity achieving codescontinues [1-4].Then in 2008, polar codes were found as the best capacity achieving code. In term s of error correcting performance, polar codes can potentially perform well as compared to the previous codes, with same code length & code rate [5].

II RELATED WORK

In this paper described about construction of polar codes .polar codes is Starting from Shannon's seminal work in 1948 [1], research on channel codes has developed for sixty years. In the past decades, the core mission of coding theory is to discover the new codes that approach Shannon limit closer than the prior codes. Motivated by this goal, information theoreticians have proposed generations of channel codes. To date, the state-of-the art channel codes are Turbo codes [2] and LDPC codes [3-4]. As the two codes that are proven to be very close to Shannon limit, Turbo codes and LDPC codes show excellent error-correcting capability, hence they have been widely adopted in numerous IEEE standards and commercial products in communication and storage systems. Although the existing capacity-approaching codes have already obtained great success in practical applications, the search for the ultimate capacity-achieving codes still continues.

The proposed decoder saves more clock cycle as the code rate increases. And high clock frequency is achieved because proposed decoder uses the data path balancing technique. Hardware complexity can be reduced by using this proposed technique.

III EXISTING SYSTEM

The channel capacity of symmetric binary input and BDMC was first achieved by using polar code[6-8]. Channel polarization phenomenon is to construct the polar code. When the data is sent on the channel with full rate channel capacity is nearer to 1 and at 0 rate data is sent through the other channels. The encoding of polar code is characterized by generated matrix and it is given as

$$G=\begin{pmatrix}1 & 0\\ 1 & 1\\ 2 & \end{pmatrix}$$

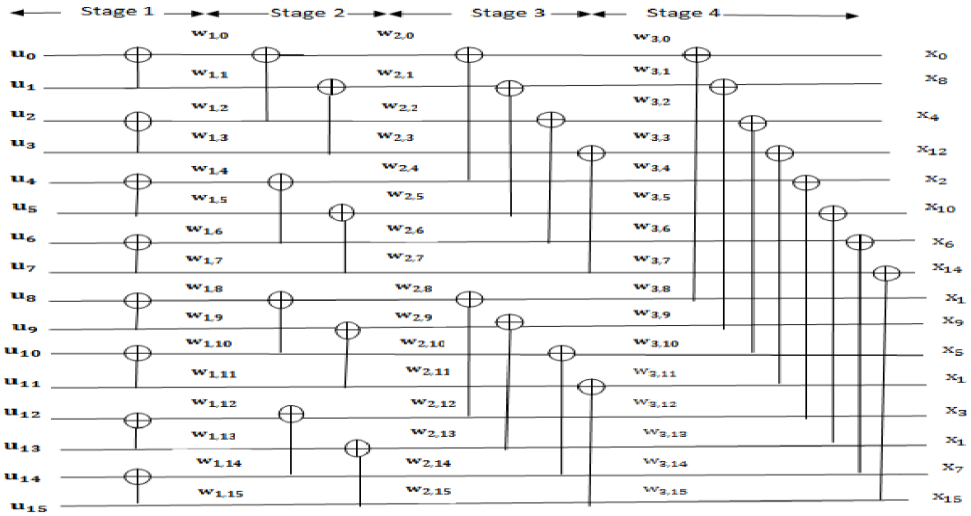

Fig.1.Design of 16 bit Fully Parallel Encoder

Fully parallel encoder architecture consists of four stages. Inputs are in natural order and output is in bit reverse order. Construction of polar code is done by using generated matrix since they belongs to linear block code. Generated matrix is represented by G. Here u and x correspond to the information and code word vectors. Codeword vector u is input arranged in natural order and x which is output codeword vector is arranged in bit reverse order. This arrangement is used to simplify the encoding process. Inputs bits are 16 and output bits are also 16. Architecture has four stages, in order to process the information, 32 XOR gates are required. The entire encoding process is accomplished in only one cycle in completely parallel encoder architecture [9],[10]. The encoder architecture design is based on generator matrix. Its implementation becomes complex as code length increases. For long polar code, it is not a suitable architecture in sort to attain the best error correcting performance. The memory size and gates required to realize the architecture increases as code length increases. In order to overcome this advantage of fully parallel architecture we go for partially parallel encoder architecture.

IV PROPOSED SYSTEM

The reduced hardware complexity an advanced architecture for long polar codes is proposed. The throughput of the proposed architecture is high therefore it can be used to design the architecture with higher level parallelism. The architecture is best suited for long polar codes [11].

FOLDING TRANSFORMATION

The folding transformation is widely used to save hardware resources by time-multiplexing several operations on a functional unit [12-16].A data flow graph (DFG) corresponding to the fully parallel encoding process for 16-bit polar codes where a node represents the kernel matrix operation F, and w_{ij} denotes the jth edge at the ith stage.

ENCODER ARCHITECTURE

Partially parallel encoder architecture design is formed by applying folding transformation to fully parallel architecture. This type of illustration is called the DFG representation. Main aim can be reduced thecomputational complexity and determined the delay. The input to the encoder is in natural order and output is in reverse order. Thestructureconsistsoffourstages.Eachstagehaseight functional units. Every node performs kernel matrix operation. V k, l represents l^{th}edge at the k^{th}stage. The designed encoder is identical to FFT. In case of the polar encoder kernel matrix operation is performed instead of butterfly computation in FFT. The encoder process 4 bits simultaneously at same time. Each function node processes two bits at a time. Thus two nodes are to processes four bits in every stage. In the folding transformation the most important designing factor is finding the folding sets. These sets represent order of the functional nodes. In that order only the operations are executed.

In order to build well-organized folding sets, the action of the encoding processes are 1^{st}divided into separate FSs. The actions of the nodes are distributed in consecutive order because the input is in natural order. Two folding sets are formed in each stage. Only even or oddoperation is performedbyeachunitofaset [17].

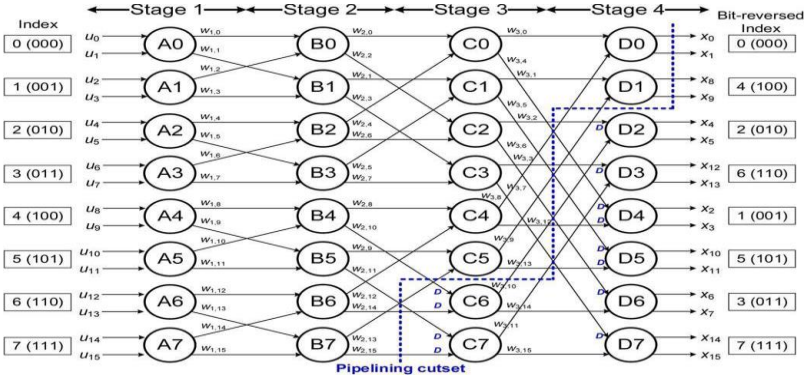

Fig.2 DFG of 16 bit polar encoding

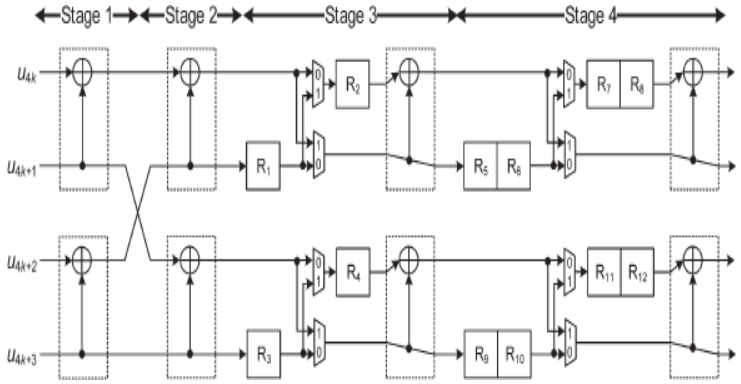

Fig.3 Proposed 4 parallel folded architecture for encoding the polar (16,k) codes

When an edge $w_{ij}$from functional unit S to functional unit T has a delay of d, the delayrequirementsforw_{ij}intheF-foldedarchitecturecanbe calculatedas

$D(w_{ij})=Fd+t-s$

whereandsdenotethepositioninthefoldingsetcorrespond- ing to T and S, respectively. Note that (1) is a simplified delay equation derived with assuming that the kernel functional unit is not pipelined. The delay requirements of the 4-folded architecture, i.e., $D(w_{ij})$ for 1 i3 and 0 <j<15, are summarized in Fig. 3. For instance, $w_{2,0}$ from B0 to C0 demands one delay since d = 0, t = 1, and s = 0.

V RESULTS AND DISCUSSIONS

In this work, partially parallel encoder has been designed and implemented using folding transformation technique. Implementation has been done using ModelSim 10.4a. Fig.4 shows the simulation result of partially parallel encoder using folding transformation technique.

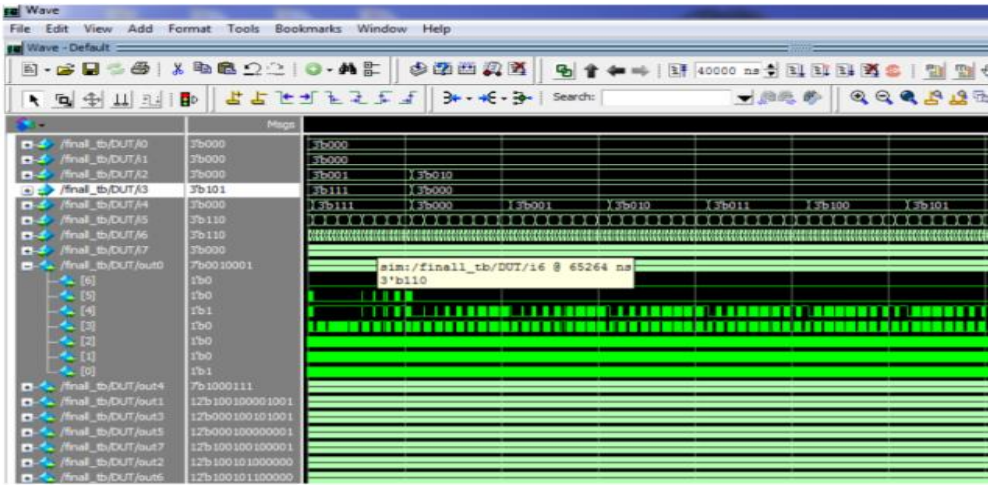

Fig.4.Simulation result of proposed system

VI CONCLUSION

In this paper, the design of partially parallel encoder has been designed using folding transformation technique. The proposed folding transformation based design are implemented using ModelSim technology. The simulation result shows that folding transformation based polar encoder consumes less power and delay compared to the existing polar encoder architecture.

REFERENCES

1) E. Arikan, "Channel polarization: A method for constructing capacity achieving codes for symmetric binary-input memory less channels," IEEE trans. vol.55, no.7, pp 3051-3073, Jul 2009.
2) I. Tal and A. Vardy, "Successive Cancellation List Polar Decoder using Log-likelihood Ratios," IEEE ISIT, pp 1-5, 2011.
3) G. Sarkis, P. Giard, A. Vardy, C. Thibeault, and W. J. Gross, "Fast polar decoders: Algorithm and implementation," IEEE J.Sel. Areas Commun, vol.32, no.5, pp.946-957, may 2014.
4) B. Yuan and K. K. Parhi, "Low-latency successive cancellation list decoders for polar codes with multi bit decision," IEEE trans. Very large scale Integration.(VLSI) Syst., DOI:10.1109/TVSLSI.2014.2359793.
5) G. Sarkis, W. J. Gross, "Polar codes for data storage applications", Proc. ICNC, pp. 840-844, 2013.
6) M.Maheswari, B. Murugeshwari, "Random and Triple burst error correction code with low redundancy for Network-on-Chip link", DOI: 10.1109/CESYS.2017.8321160 (IEEE XPLORE)
7) N. Radha and M. Maheswari, "High Speed Efficient Multiplier Design using Reversible Gates," 2018 International Conference on Computer Communication and Informatics (ICCCI), Coimbatore, 2018, pp. 1-4. doi: 10.1109/ICCCI.2018.8441326 (IEEE Xplore)
8) G.S. Sankari, M. Maheswari, "Energy Efficientweighted Test Pattern Generator Based BIST Architecture", I-SMAc-2018-IEEE Xplore- 2018.
9) N. Radha and M. Maheswari ," An Efficient Implementation of BCD to Seven Segment Decoder using MGDI", I-SMAc-2018-IEEE Xplore- 2018.
10) M. Banupriya, M. Maheswari," Multicarrier Modulation For 5g Mobile Applications", IOSR Journal of Electronics and Communication Engineering (IOSR-JECE), pp. 1-5.
11) K.Vigneshwaran, T.Muruganantham,"Low Complexity Matrix Inversion Algorithm for Throughput Data Detection in the Hyper MIMO Reverse Channel" International Journal of Applied Engineering Research, Vol 1, Issue 2, Nov 2014.
12) K.Vighneshwaran, T.Muruganantham, **"**High Performance Hardware for data detection in Single Carrier Frequency division multiple access (SC-FDMA) based massive MIMO", International Journal of VLSI and Signal Processing, 2014.

13) B.I.S.Ronica, B.Murugeshwari, "OHWDM based Modulation Comparison For Minimum Bit Error Rates" International journal of recent advances in science and engineering vol 1 issue 1 march 2015, pp. no 95-98.
14) G.Gomathi, S. Rajapriya, **"**Energy Improved Node Disjoint Multipath Routing Protocol for Wireless Sensor Network", Vol. 120, No. 6, July 9, 2018
15) K.Abinaya, "Design of Compact Bandpass Filter using Open Stubs Loaded Shorted Stepped Impedance Resonator with High Band to Band Isolation" SSRG International Journal of Industrial Engineering, Vol. 1, Issue 4, Oct 2014.
16) Revathi, A Jeyalakshmi, C "Robust Speech Recognition in Noisy Environment using Perceptual Features and Adaptive Filters", Proceedings of 'International Conference on Communication and Electronics Systems (ICCES 2017), IEEE explore, pp.692-696, 2018.
17) Revathi, A Jeyalakshmi, C Muruganantham, T "Perceptual Features based Rapid and Robust Language Identification System for Various Indian Classical Languages", In: Hemanth D., Smys S. (eds) Computational Vision and Bio Inspired Computing. Springer Lecture Notes in Computational Vision and Biomechanics book series (LNCVB), vol. 28, pp.291-305,2018.