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A NOVEL DOUBLE GATE JUNCTION-LESS MOSFET USING GERMANIUM

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ABSTRACT:

In this paper, a novel Double gate junctionless MOSFET is proposed using germanium as the channel material. In early days germanium was mainly used for the fabrication of semiconductor devices, but due to its high leakage current it was unsuitable for high temperature applications though its mobility is higher than silicon. So to overcome this problem a high- k dielectric gate oxide such as HfO_2 is used. The performance of 16-nm germanium symmetric double-gate junctionless transistor (Ge-DGJL T) is evaluated and compared with different gate materials and analysis has been carried out by using 2D- Cogenda Visual TCAD simulator. The performance parameters, such as drain current (Id), threshold voltage (Vt), drain induced barrier lowering (DIBL), subthreshold slope (SS), are systematically investigated for n-type Ge-DGJLT.

KEYWORDS: Double-gate junctionless transistor (DGJLT);DIBL; scaling; subthreshold slope.

INTRODUCTION:

Over the last decade size of CMOS Devices reduce exponentially. It helps to increase operating speed of circuit, improves the number of transistor on chips and ultimately reduce the manufacturing cost per chip. The process of reducing overall dimension of device is known as scaling. Scaling of conventional Metal Oxide Semiconductor Field Effect Transistor (MOSFET) required shallow doping at source and drain region, this process becomes more complicated and degrade the performance of device when scaling reach to sub 30 nm regime. Due to the rapid shrinking of MOSFETs, semiconductor industries face drastic challenges in the formation of source and drain junctions in short-channel devices.

To overcome these challenges, a novel source-channel and drain-channel junction free transistor structure is proposed called junctionless transistor (JLT). Junctionless transistor has uniform doping concentration over source-channel-drain region. It has many advantages over conventional MOSFET's such as high scalability, simple process flow, low thermal budget, improved performance against short channel effects. Furthermore, Ge as a high mobility material has been reported to be a promising candidate as channel material for future devices. Some studies on Si junctionless nanowire transistors can be found in the literature.

In this dissertation work, design and simulation of a novel JLT with Germanium as channel material and Hafnium dioxide as gate oxide has been carried out. A comparative analysis with respect to various performance measuring parameters namely; sub-threshold swing (SS),drain induced barrier lowering (DIBL), current ratio, static power dissipation. The process parameters considered for simulation are channel physical gate length (L_G), and gate oxide material (SiO_2, Si_3N_4, HfO_2). Extensive 2-D simulations have been carried out in Cogenda Visual TCAD simulator. Simulation results show that incorporating Germanium as a channel material in place of silicon with HfO_2 as gate oxide material improves gate leakage current, operating speed and performance parameters of the proposed device. This is mainly due to high mobility of Germanium. It has been found that by incorporating high-k material such as HfO_2 as gate oxide short channel effects in JLT reduces. This shows improvement in the figures of merits of proposed JLT over other device structures.

LITRATURE REVIEW:

The literature survey focus on a non-classical structure called Junctionless Transistors, various research groups are work on the projects to improving its performances and reducing the cost. The various approaches used in the literature are,

J. P. Colinge [1] become first to invent and describes the physics and basic properties of Junctionless transistors.It was found that SOIJLT hasless

subject to short-channel effects than devices with junctions. However, the fabrication process is simple with low thermal budget. SOIJLT shows excellent subthreshold slope and drain induce barrier leakage.

A. Kranti et al., [2] describe the fabrication of Junctionless nanowire transistor (JNT) on Bulk Silicon. The devices have advantages like simple process flow, low thermal budget. JNT behave as regular multi-gate SOI transistors, and less affected to short-channel effects than conventional MOSFETs. Further, describes the conduction mechanisms in JNT and compared with inversion-mode and accumulation-mode MOS devices.

C-H Tai et al.,[3] proposed A Novel structure of Junctionless transistors for High-Performance on Bulk-Si Wafer called Junctionless Vertical MOSFET.

J. P. Colinge et al.,[4] describes the basic properties and physics of Junctionless transistors, and compares Junctionless transistors with inversion-mode devices.

S. Gundapaneni et al., [5,6] proposed a novel device structure on bulk silicon called bulk planar Junctionless transistor (BPJLT) enhanced electrostatic properties of Junctionless Transistor with High-*k* spacer, it shows increase in electrical gate length of device in the OFF-state.

R. K. Baruah et al., [7, 8, 9] reported an better analog performance BPJLT compared with SOI JLT. Furthermore comparison carried between silicon and germanium Junctionless Double-Gate Field Effect Transistor which gives germanium DGJLT is having better performance as compared to silicon DGJLT for digital and analog applications.

Lou H., Lining Zhang, Yunxi Zhu, Xinnan Lin, Shengqi Yang, Jin He, Chan M.,[10] demonstrated characteristic of a dual-material-gate junctionless nanowire transistor (DMG-JNT).

Rudenko T., Yu R., Barraud S., Cherkaoui K., Nazarov A.,[11] proposed a new method to extract the doping concentration and flat-band voltage in junctionless (JL) multi-gate nanowire (NW) MOSFET based on using the gate-to-channel capacitance measurements of devices with different relatively small NW widths.

DEVICE STRUCTURE AND SIMULATION:

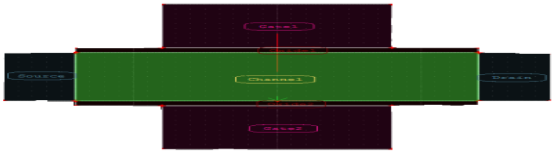

Fig 1. Crosssectional view of DGJLT using Ge for physical channel length,L_D=16nm.

The device structure used for this study namely Ge-DGJLT is shown in Fig.1. A junctionless transistor (DGJLT) has no p-n junction in the source-channel-drain path. An n-type device have an N+- N+ -N+ structure and p-type device have a p+-p+-p+ doping for the source, channel and drain region respectively.

Electrical characteristics for the devices simulated for process/device parameters as shown in table 1 using 2D Cogenda Visual TCAD simulator. For all the simulations, uniform channel doping concentrations taken throughout the channel, source/drain regions.

Table 1: Process /Device Parameters

Parameters	Value
Channel Doping , N_D	$2*10^{19}$ cm^{-3} (N type)
Gate Workfunction: For SiO_2 For Si_3N_4 For HfO_2	 5.047eV 4.791eV 4.62eV
Gate oxide thickness, T_{ox}	1 nm
Substrate thickness, T_{Ge}	10 nm
Physical gate length, L_D	16-45 nm

SIMULATION RESULTS:

Fig.2 shows simulated I_{DS}-V_{GS} characteristics of n-type Germanium DGJLT for different gate oxide materials with V_{DS}=50mV and L_D= 16nm. The off-state current I_{OFF} when V_{GS}=0V and V_{DS}=1V is minimum when we use HfO_2 as gate oxide as compared to others, since the dielectric constant is high for HfO_2(22) as compared to SiO_2(3.9)and Si_3N_4(7.5).

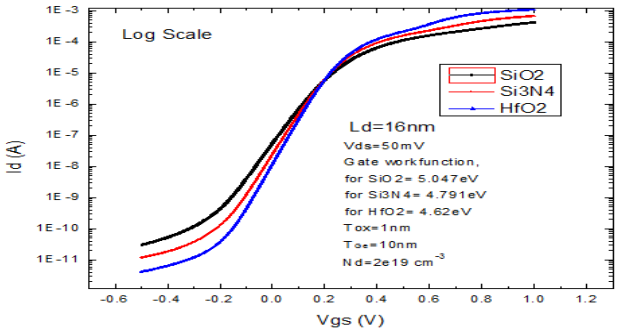

Fig.2 I_D-V_{GS} Characteristics of Ge-DGJLT with V_{DS}=50mV for L_D=16nm.

Fig. 3 shows the variation of DIBL with physical gate length for all the devices. The DIBL for Ge-DGJLT with gate oxide material SiO_2,Si_3N_4 and HfO_2 are 130.52mV/V, 70.52mV/V, 40mV/V respectively for L_D=16nm .

The DIBL isthe difference between threshold voltages when gate voltage is increased from 50 mV to 1 V (DIBL=Vt (V_{DS}=50 mV)- Vt (V_{DS}=1V)) [9]. The DIBL is better for Ge-DGJLT with HfO_2 as gate oxide materials.

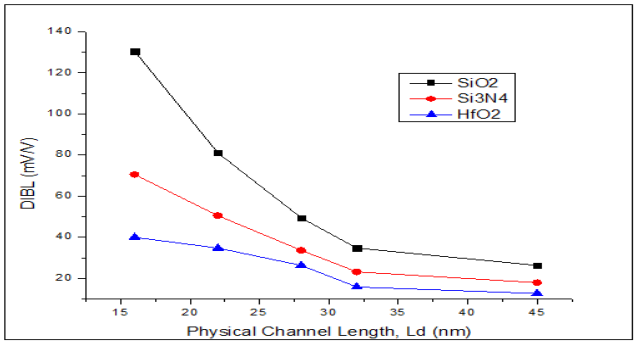

Fig. 3 Variation of DIBL with physical gate length L_D=16nm-45nm.

Fig. 4 shows variation of sub threshold slope (SS) with physical channel length all the devices. The subthreshold slope for Ge-DGJLT with gate oxide material SiO_2,Si_3N_4 and HfO_2 are 246mV/dec, 192mV/dec and 159mV/dec respectively for channel doping concentration, N_D=2x$10^{19}cm^{-3}$. The subthreshold slope is the variation in gate to source voltage (V_{GS}) for one decade change in drain current in the subthresholdregion[4]. The lesser value of SS for Ge-DGJLT with HfO_2 gate oxide will make the switching time between I_{ON} and I_{OFF} lesser as compared to others. So the device performance is faster.

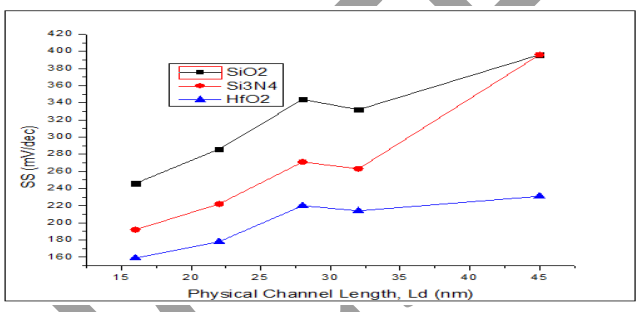

Fig. 4 Variation of SS with physical gate length L_D=16nm-45nm.

Fig. 5 shows the variation of static power dissipation with physical channel length all the devices. As I_{OFF} is minimum for the Ge-DGJLT with HfO_2 than SiO_2 and Si_3N_4, the static power dissipation is also minimum for Ge-DGJLT with HfO_2 (P_{STAT}=I_{OFF}*V_{DS}). It means that, power consumption is low so thermal budget is minimum,so no need of heat sinks required.

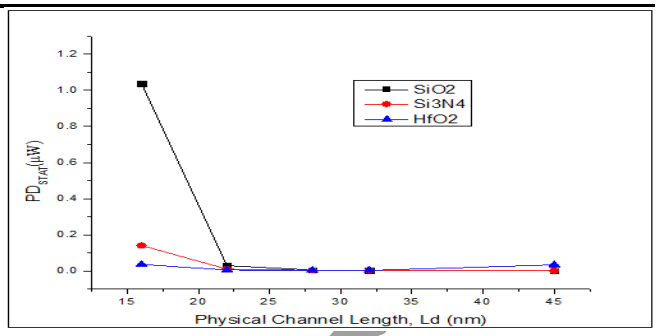

Fig. 5 Variation of static power dissipation with physical gate length L_D=16nm-45nm.

CONCLUSION:

In this work, a novel Double gate junctionless MOSFET using germanium as the channel material and high- k dielectric material HfO_2 as gate oxide with physical channel length 16nm is proposed. A comparative analysis with respect to various performance measuring parameters namely; sub-threshold swing (SS),drain induced barrier lowering (DIBL), drain current, static power dissipation for Ge-DGJLT with SiO_2, Si_3N_4 and HfO_2 as gate oxide materials. The Ge-DGJLT with HfO_2 as gate oxide material shows the overall better performance with respect to others.

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