Proceedings of
INTERNATIONAL CONFERENCE ON INNOVATIVE TRENDS IN ENGINEERING RESEARCH (ICITER-2016)
International Journal of Innovations in Engineering, Research and Technology,IJIERT-ICITER-16,ISSN:2394-3696
26th June,2016

OVERVIEW OF POWER OPTIMIZATION TECHNIQUES IN WIRELESS PERSONAL AREA NETWORK

[PAPER ID: ICITER-C116]

RAMESH Y. MALI
Shri Jagdishprasad Jhabarmal Tibrewala University ,
Vidyanagari, Dist. Jhunjhunu, Rajasthan (India)– 333001

DR. PRADEEP B. MANE
Principal, A.I.S.S.M.S., Institute of Technology, Pune, Maharashtra

ABSTRACT:

A low power CMOS based RF transceiver architectures are proposed with the gigahertz frequency for the applications in the field of the industrial, scientific and medical .The integrated circuit (IC) is fabricated by using CMOS 0.18 technology. The circuit consists of the RF receiver, RF transmitter and the synthesizer with the on chip oscillator. These proposed chips are fully complies with the wireless personal area network standard nothing but IEEE 802.15.4 which is for low power consumption. The various specifications are compared such as noise figure, current consumption, sensitivity, IIP3, percentage EVM. The proposed chips used ultra low 1.8 V power supply with 29mW power consumption for transmitter and 23 mW for reception mode.

INDEX TERMS: ***CMOS, integrated circuit (IC), low power, RF transceiver, Wireless personal area networks (WPANs), IEEE 802.15.4***

INTRODUCTION:

THE IEEE 802.15.4 STANDARD:

A low power (rate) wireless personal area network (LR-WPAN) is kind of the wireless network which is specially designed for the low cost low power short range of wireless networks. Higher data throughput is the necessary specifications of the wireless communication network but for the smaller range wireless network requires the relaxed throughput and the latency requirement. The IEEE 802.15 working group defined the standard for the Low power wireless personal area network LR-WPAN nothing but IEEE 802.15.4. This standard is specifically designed for the industrial residential and medical purpose where the power consumption is very low and cost also with the relaxed the data rate and QoS (Quality of Service). This standard is very useful for the POS (Personal Operating Space) with large number of wireless of nodes.

Specifications	WLAN	BT based WPAN	Low Rate WPAN
Range	Up to 100m	Approx.10 to 100m	10m
Data throughput	Up to 2 to 11Mb/s	1Mb/s	<0.25Mb /s
Power consumption	Medium	Low	Ultra Low
Size	Larger	Smaller	smallest
Cost/complexity	>6	1	0.2

Table 1: A comparison of LR-WPAN with other wireless technologies

Characteristics of the LR-WPAN are different than the other WPAN. The most important characteristics of the LR-WPAN is the data throughput of the network which having the range from the few bits to the few kilobits per seconds. Low data rate and low power consumption of LR-WPAN are also the different characteristics with various variable network topologies. Some system design criteria are specified for IEEE standard of LR-WPAN. Reductions in the some variables of the system design are mentioned as below for the achievement of low power consumption so as to increase the battery life of the system.

1. The amount of data transmitted
2. The Trans-receiver duty cycle and frequency for the transmission of data
3. Frame overhead

Technically, implementation of mechanisms for the power management like sleep modes and power –down of the system lead to less power consumption.

Techniques to implement the power optimization for the LR-WPAN:

1. 2.2 GHZ CMOS INTEGRATED RF TRANSCEIVER FOR WPAN :

For industrial, scientific and the medical applications of WPAN with low power capability a CMOS integrated RF transceiver is designed for the gigahertz frequency. The integrated circuit is designed so as to fulfill the specifications of the WPAN standard IEEE 802.15.14. System architecture is designed or proposed for the WPAN for the achievement of the low power and low cost specifications of the network. The architecture consists of the RF transceiver and a frequency synthesizer with VCO (voltage controlled oscillator).Here in this proposed low power and low cost architecture of transceiver contains 6 bit DAC and 4 bit ADCs. The overall architecture of the sub-gigahertz RF transceiver is as follows.

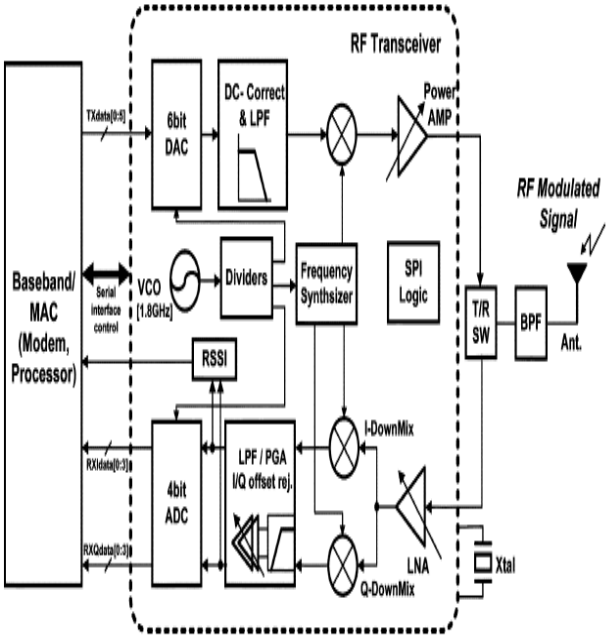

Figure 1: RF transceiver architecture with the baseband processor

In above architecture, the RF signal with GHz frequency is amplified by a LNA (a low noise amplifier) and converted to zero –IF I/Q signal. For this, two identical mixers are used which are driven by signals from the frequency synthesizer i.e. LO signals. In the next analog baseband stage the channel filtration, signal amplification and the dc offset cancellation is done through filter and programmable gain amplifier. Generation of the baseband BPSK signal is done through the MODEM block in the architecture followed by the 6 bit DAC. RF transceiver integrated circuit is designed with above specifications like 0.18-µm mixed-signal CMOS which includes the 6 metal layers of 2 µm of thick top metal provides good quality factor with high gain, results into the low power consumption in given RF and analog circuits. This chip requires 1.8 V operating power supply with very less power consumption of 25mW for reception mode and 29 mW for the transmission mode[1].

2. 2.4 GHz an ultra low power CMOS Integrated RF Transceiver for WPAN:

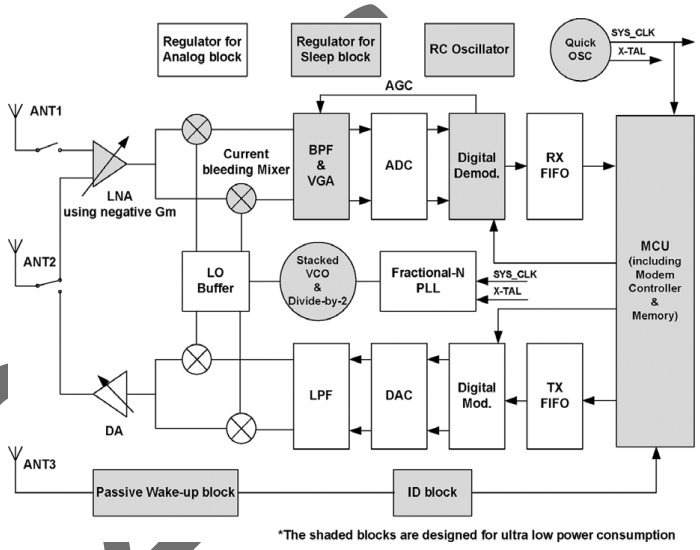

Figure 2: A proposed model for the 2.4 GHz CMOS RF Transceiver

The above proposed model for RF system is designed to achieve low power consumption like direct conversion (zero-IF), Low-IF, architectures with sigma delta ADC, the polar transmitter and the sub sampling receiver. The architecture consists of the digitized receiver to receive the multi-standard signals in order to save the power consumption. The receiver is of the SD-ADC sub sampling type. The polar type of transmitter of the architecture replaces the DAC and the up-conversion mixer so as to reduce the power consumption. But, it requires the control circuits in massive structure to match the delay and the amplitude. In this proposed super heterodyne architecture the low-IF receiver and the direct conversion transmitter are used for the good quality performance with high level of integration and the low power. The shaded blocks in the proposed architecture like VCO, LNA, Oscillator, Wake-up block and regulator are implemented particularly to achieve the low power consumption of 1.8 V [2].

Comparison of various specifications of Transceiver technology based on the CMOS fabrication with 0.18 µm for the low power low cost WPAN. Following is the detailed tabular form of various specifications requires designing the low power CMOS transceiver for the WPAN.

Table: Comparison Results for the various Transceivers Technology

Specifications	2.2GHz CMOS RF	2.4 GHz CMOS ZigBee
Process	0.18-µm	0.18-µm
Power Input	1.8V	1.8V
Output (GHz)	2.2 GHz	2.4 GHz
Current Consumption	25-29mA	14.3 – 16.7 mA
Noise Figure	9.5 dB	-
Sensitivity	-98dBM	-101dBM
IIP3	-10dBM	-11dBM
% EVM	6.3	Less than 5

CONCLUSION:

This paper presents the overview of various proposed models of power optimization techniques in wireless personal area network. Various researchers have identified the scope for power optimization techniques. Secure communication models are needed due to rapidly growing wireless area networks. A fast responding system with lowest losses is a need of time. IEEE 802.15.4 Standards are also discussed in the paper.

REFERENCES:

i. Seo, Hae-Moon, et al. *"A low power fully CMOS integrated RF transceiver IC for wireless sensor networks."* Very Large Scale Integration (VLSI) Systems, IEEE Transactions on 15.2 (2007): 227-231.

ii. Kwon, Yong-Il, et al. "*An ultra low-power CMOS transceiver using various low-power techniques for LR-WPAN applications."* Circuits and Systems I: Regular Papers, IEEE Transactions on 59.2 (2012): 324-336.

iii. Gutierrez, Jose A., et al. *"IEEE 802.15. 4: a developing standard for low-power low-cost wireless personal area networks."* network, IEEE 15.5 (2001): 12-19.

iv. Paschalidis, Ioannis Ch, Wei Lai, and David Starobinski. *"Asymptotically optimal transmission policies for large-scale low-power wireless sensor networks."* Networking, IEEE/ACM Transactions on 15.1 (2007): 105-118.

v. Hui, Jonathan W., and David E. Culler. "*Extending IP to low-power, wireless personal area networks."* Internet Computing, IEEE 12.4 (2008): 37-45.

vi. Saad, Mohamed. *"Optimal spectrum - efficient routing in multichip wireless networks*." Wireless Communications, IEEE Transactions on 8.12 (2009): 5822-5826.

vii. Khan, Nawreen, Masum Hossain, and KL Eddie Law. "*A low power frequency synthesizer for 60-GHz wireless personal area networks*." Circuits and Systems II: Express Briefs, IEEE Transactions on 58.10 (2011): 622-626.

viii. Li, Geoffrey Ye, et al. "*Energy-efficient wireless communications: tutorial, survey, and open issues.*" Wireless Communications, IEEE 18.6 (2011): 28-35.

ix. Samaras, Ioakeim K., George D. Hassapis, and John V. Gialelis. "*A modified DPWS protocol stack for 6LoWPAN-based wireless sensor networks.*" Industrial Informatics, IEEE Transactions on 9.1 (2013): 209-217.

x. Amin, Osama, and Lutz Lampe. "*Opportunistic energy efficient cooperative communication."* Wireless Communications Letters, IEEE 1.5 (2012): 412-415.

xi. Sohyeong Kim, Ilku Nam, Taewook Kim, Kyucheol Kang, and Kwyro Lee, *—A Single-Chip 2.4GHz Low-Power CMOS Receiver and Transmitter for WPAN Applications‖.*

xii. S. V. Kishore, Glenn Chang, and Chris Hull —A SOI-Bi-*CMOS RF-Transmitter for Personal Digital Cellular Communication (*PDC)‖,Silicon Wave Inc., 6256 Greenwich Dr., Suite 300, San Diego; CA 92122-5941, USA ,Symposium on VLSl Circuits Digest of Technical Papers , PP. 60-65,2000 IEEE.

xiii. Seok-Bong Hyun, Geum-Young Tak, Sun-Hee Kim,Byung-Jo Kim, Jinho Ko, and Seong-Su Park *—A Dual-Mode 2.4-GHz CMOS Transceiver for High-Rate Bluetooth Systems‖.*

xiv. Theodore S Rappaport —*Wireless Communications‖ Principles and Practice Pearson Education* India.

xv. T. L. Singal —*Wireless Communications‖, Tata McGraw-Hill Education.*

xvi. Yao-Hong Liu, Cheng-Lung Li, and Tsung-Hsien Lin, —A 200-pJ/b *MUX-Based RF Transmitter for Implantable Multichannel Neural Recording‖*, IEEE Transactions on Microwave Theory and Techniques, Vol. 57, No. 10,PP- 2533 -2541, October 2009.

xvii. Yahia Tachwali, Hazem Refai —*Implementation of a BPSK Transceiver on Hybrid Software Defined Radio Platforms‖,* University of Oklahoma, Department of Electrical & Computer, Engineering