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An overview of Adaptive Binary Range Coder with low memory requirement

Sharda B. Shelke, PG Student

Department of E&TC

STES'S, Smt.Kashibai Navale College of Engineering

Sr. No. 44/1, Off. Sinhgad Road,

Vadgaon (Bk), Pune-411041, India.

sharda.shelke93@gmail.com

Prof. Anjali .A. Yadav

Department of E&TC

STES'S, Smt.Kashibai Navale College of Engineering

Sr. No. 44/1, Off. Sinhgad Road,

Vadgaon (Bk), Pune-411041, India.

rasalanjali@gmail.com

Abstract⸺ There are number of coders used in video or image compression techniques such as MQ-coder used in JPEG2000, Q-coder used in JPEG. In proposed system, the virtual sliding window is used for probability estimation, which does not uses lookup table. For improving compression performance a new adaptive window size selection algorithm is used. As compared to the binary range coder with a single window, the proposed algorithm provides a faster probability estimation and adaptation at the initial encoding and decoding stage, and more precise probability estimation for very low entropy binary sources. In proposed system uses virtual sliding window, therefore the memory requirement is less as compared to previous system. The power consumption of proposed system is measured by using the Xilinx Xpower analyzer. The power consumption is reduced in proposed Adaptive Binary Range Coder as compared to previous coders like M-coder and MQ-coder.

Keywords⸺*Arithmetic coding, image and video compression, range coder, Entropy coding, FPGA, HDL.*

I. INTRODUCTION

Adaptive binary arithmetic coding plays an important role in various video and image compression standards, such as JPEG, JPEG2000, H.264 which is AVC (Advanced Video Coding), and H.265 which is HEVC standard (High Efficiency Video Coding). In proposed system computational complexity is considered as a key bottleneck in video or image compression standards, For implementation of efficient hardware and software great efforts are required. In previous architectures, the cost of multiplication has been very much higher than the architecture which uses lookup tables. Therefore, the first fast Adaptve Binary Arithmetic Coder (ABRC) implementation, called Q-coder and its followers use lookup tables for probability estimation and approximation of the multiplication operation in the interval division part and bit renormalization, which makes this approximation possible. Range coders are an alternative to arithmetic coders, which uses bytes as output bit stream elements and perform byte renormalization at a time. Adaptive binary range coder (ABRC) can be efficiently used for image and video coding as well as for data compression [1]. For software implementation, it was shown that ABRC achieves up to 40% less computational complexity compared with the M-coder. However, from a hardware implementation point of view, the main drawback of ABRC is the use of a multiplication in the interval division part [1]. On the other hand, in modern architectures, the cost of multiplication can be comparable with the cost of using a lookup table. In this paper, it presents a hardware-efficient ABRC. The main contributions of this project are the following.

1).The new Adaptive binary range coder (ABRC) system is a modification of adaptive binary range coding, which gives efficient hardware implementation. This system shows how to reduce the bit capacity of the multiplication which needed in the interval division part and it shows how to avoid a loop usage in the renormalization part of ABRC.
2). The ABRC system uses VSW (virtual sliding window) for probability estimation, which does not use lookup tables. To achieve a higher compression performance, a new adaptive window size selection algorithm is proposed. In comparison with the a single window ABRC architecture, the proposed Virtual sliding window algorithm provides a faster probability adaptation at the initial encoding and decoding stage and it also gives more precise probability estimation for very low entropy binary sources.
3).It introduces a VLSI (Very-Large-Scale Integration) architecture of the proposed ABRC and shows that it provides comparable throughput in comparison with MQ-coder (used in JPEG2000) and M-coder (used in H.264/AVC and H.264/HEVC) and a higher throughput in comparison with the existing ABRC . In the proposed ABRC system it does not use any additional memory block such as lookup tables and it consumes very less power than the other coders.

Department of Electronics & Telecommunication, Marathwada Mitra Mandal's College of Engineering, Karvenagar, Pune-52

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II. RELATED WORK

Adaptive binary arithmetic coding plays an important role in various video and image compression standards, such as JPEG, JPEG2000, H.264 which is AVC (Advanced Video Coding), and H.265 which is HEVC standard (High Efficiency Video Coding). In proposed system computational complexity is considered as a key bottleneck in video or image compression standards, For implementation of efficient hardware and software great efforts are required. In previous architectures, the cost of multiplication has been very much higher than the architecture which uses lookup tables. Therefore, the first fast Adaptve Binary Arithmetic Coder (ABRC) implementation, called Q-coder and its followers use lookup tables for probability estimation and approximation of the multiplication operation in the interval division part and bit renormalization, which makes this approximation possible.

In the technique presented in [2] was a new adaptive window size selection algorithm for efficient probability estimation in binary range coder. The proposed algorithm based on three-dimensional discrete wavelet transform was embedded in low-complexity video codec. Simulation results shows that for the 3-D DWT codec the proposed algorithm provides increase in quality for a given bit rate and the computational complexity increase from 1.4 to 2 times. Compared to fast software implementation of the H.264/AVC standard (x264 codec in ultrafast mode) The modified 3-D DWT is from 1.6 to 5 times less complex for the same quality level. Therefore, it is more preferable than H.264/AVC if the system requires a low-complexity scalable video coding techniques. There exist video transmission and coding applications, like video coding on mobile devices, video transmission for WSN (wireless sensor networks), 3D videoconferencing, wireless endoscope capsules, and so on, in which video encoding, decoding, video capturing , packet loss protection and playback should operate in real-time and computational resources (or power consumption) for encoding are very restricted. At the same time, during transmission the video bit stream rate must be easily varied at the encoder side, and it should be easily truncated at any intermediate network node for adaptation to the channel bandwidth at the current link and or end-user display. A SVC (low-complexity scalable video coding) is the most preferable compression method for applications mentioned above. However, the most popular SVC approach based on H.264/AVC standard requires relatively a high computational resources which is a significant barrier for its use for these applications. In previous work proposed a scalable video coding algorithm based on three-dimensional discrete wavelet transform (3-D DWT) which is low-complexity technique. It was shown that compared to the H.264/AVC standard in the low complexity mode the proposed 3-D DWT video codec has a much lower computational complexity (from 2 to 6 times). However, in some cases, its rate distortion performance can be lower than H.264/AVC (up to 2 dB). To improve the coding performance of the 3-D DWT codec, in this paper for efficient probability

estimation in binary range coder auther proposes a new adaptive virtual sliding window size selection algorithm, which is a core part in wavelet subband bit-plane entropy encoder. It show that the modified 3-D DWT codec for a given bit rate provides significant quality increase. Compared to the computational complexity of a fast software implementation of the H.264/AVC standard the computational complexity of this system is very less .

a novel efficient adaptive binary arithmetic coder which is multiplication-free and it does not requires look-up tables which is proposed in [4]. To achieve this, it combines the probability estimation based on a virtual sliding window with the approximation of multiplication and the use of simple operations to calculate the next approximation after the encoding of each binary symbol. We show that in comparison with theM-coder the proposed algorithm provides comparable computational complexity, less memory Adaptive binary arithmetic coding (ABAC) is an essential component in most common image and video compression standards and several non standardized codecs such as JPEG, JPEG2000, H.264/AVC, HEVC and Dirac. Arithmetic coders implemented in these codecs are based on the so called Q-coder [6] which is a multiplication-free adaptive binary arithmetic coder with a bit renormalization and look-up tables used for multiplication approximation and probability estimation. The most efficient ABAC implementation is the M-coder, which is the core of the Context-adaptive binary arithmetic coding (CABAC) used in the H.264/AVC standard. The emerging HEVC standard,also uses the M-coder as an encoding engine in CABAC, but in contrast with H.264/AVC the context-modeling in HEVC is significantly simplified. Therefore,the computation complexity and memory consumption portions of the M-coder in CABAC of HEVC are higher than those in H.264/AVC footprint [4].

III. PROPOSED METHODOLOGY

Adaptive binary arithmetic coding plays an important role in various video and image compression standards, such as JPEG, JPEG2000, H.264 which is AVC (Advanced Video Coding), and H.265 which is HEVC standard (High Efficiency Video Coding). In proposed system computational complexity is considered as a key bottleneck in video or image compression standards, For implementation of efficient hardware and software great efforts are required. In previous architectures, the cost of multiplication has been very much higher than the architecture which uses lookup tables. Therefore, the first fast Adaptve Binary Arithmetic Coder (ABRC) implementation, called Q-coder and its followers use lookup tables for probability estimation and approximation of the multiplication operation in the interval division part and bit renormalization, which makes this approximation possible.

A.Proposed Block Diagram

Fig. 1 shows block diagram of proposed system. Camera is used for video or image input. The video or image

input is given to Matlab which is used to convert it into binary format. When any image is given as input to matlab then at workspace we get its binary equivalent sequence. This binary input is given to Xilinx platform through the verilog or VHDL coding. By using synthesis report we can calculate memory requirement for a proposed encoder. In Xilinx there is inbuilt Xpower analyser.
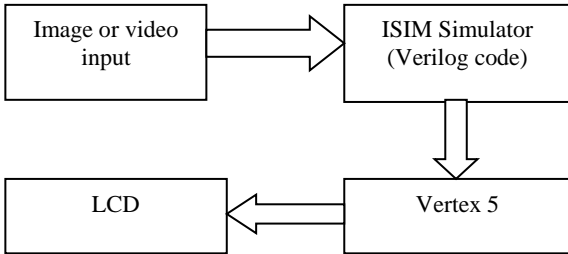

Fig.1 Proposed system block diagram
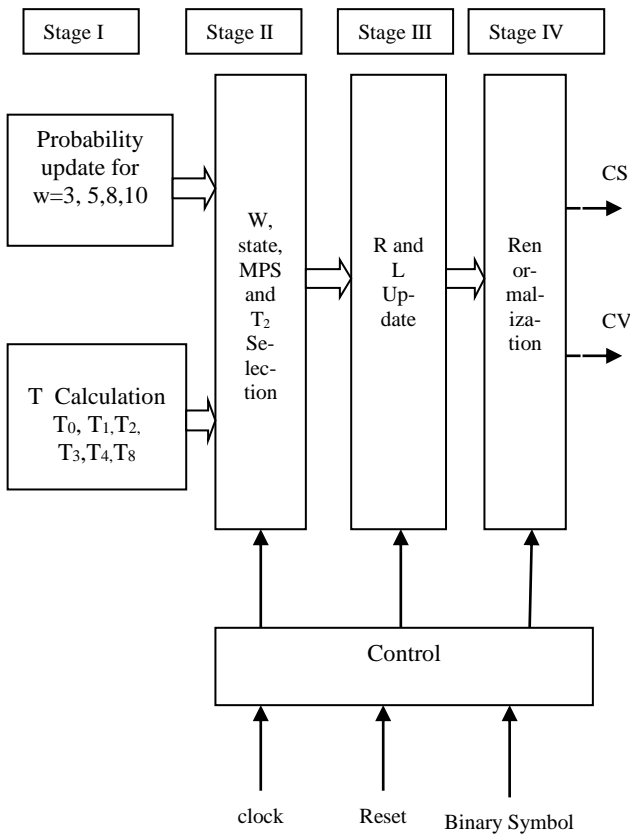
B. General Scheme of adaptive binary range coder

Fig.2 General scheme of adaptive binary range coder

The general scheme of the proposed ABRC hardware architecture is shown in Fig.2, which consist of four processing stages. After reset is stable, the ABRC system is ready to receive an input which is binary symbol, which is driven by the clock signal.

At the first stage, the new probability estimation values are calculated by using four probability updating windows operating in parallel for $W = 2^3$, 2^5, 2^8, and 2^{10}. Each core calculates the values of window size 2^w, most probable symbol (MPS), state s, (w, s) and T_2 for the next binary symbol at the same time, the six different T values generated by T calculation circuit .

At the second stage, one value of T is selected from the six values depending on the a new window size 2^w with the corresponding variables are selected for the next binary symbol and value of (w, s).

At the third stage, registers L and R as well as H (temporal register) are updated .

At the fourth stage, the part of renormalization is triggered by the output of the upper eight bits of register L and H. The cv, cs output bit stream interface is employed: cv stands for a code valid signal which is 1 bit in length while cs stands for a code stream with a width of 8 bit. At last, a control module is configured for whole encoding processing of the system.

C. Detailed ABRC architecture

Detailed ABRC architecture is shown in fig. 3, in which fig. 3(a) shows probability updation for input symbol. This circuit is for window size w=5. It uses adder, left shift operators ,right shift operators, Multiplexers for performing different operations.The output bits of probability updation is given to T selection block of encoder.
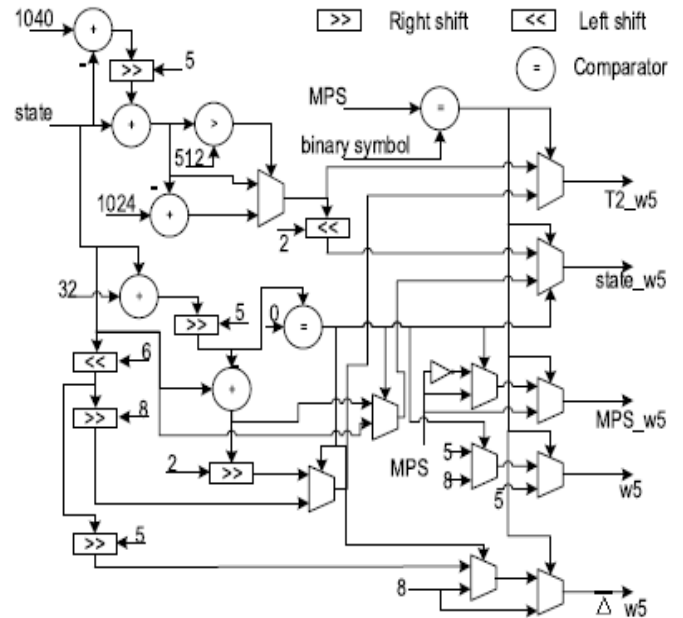

Fig. 3.(a)Probability updation.[1]

Fig. 3(b) shows internal logic for selection of T,state, MPS depending on the values of window size w. similar to

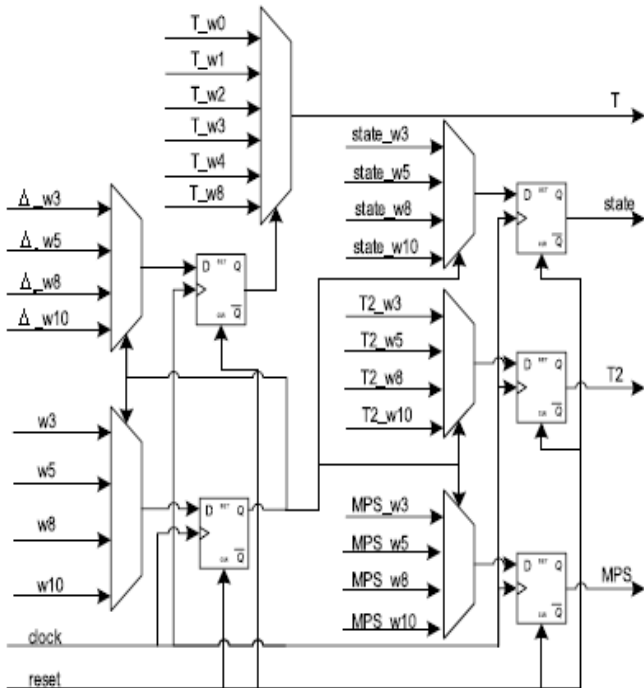fig. 3(a) ,Fig. 3(b) also uses different logic operators for performing T selection.

Fig. 3.(b) MPS,T,T_2,State selection.[1]

As shown in Fig, At the output of fig.3(b) it gives selected parameters like T,State,T_2 and Most probable symbol(MPS) .
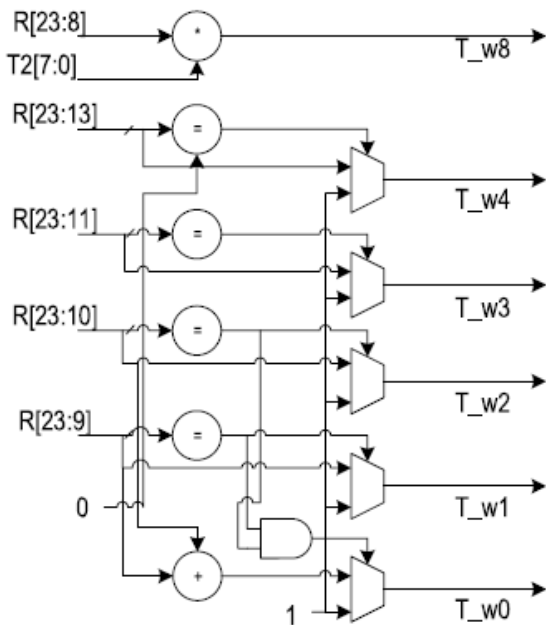
Fig. 3(c) shows architecture of T calculation of input symbol. It designed by using basic logic blocks like adder,comparator, and gate and multiplexers.

Fig. 3(d) shows internal logic for R,L and H updation. Fig. 3(e) shows internal structure used for renormalization for L and R which are internal variable and Fig. 3(f) shows logic for byte output stream.
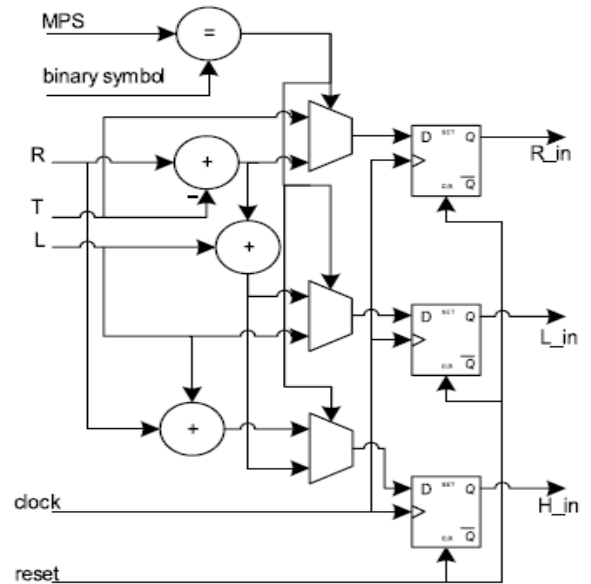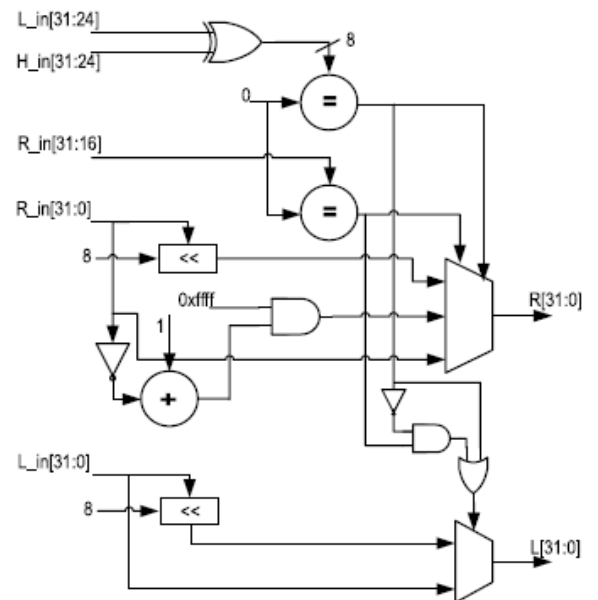

Fig.3(d)Updation of R and L [1].

Fig.3(c) T Calculations [1].
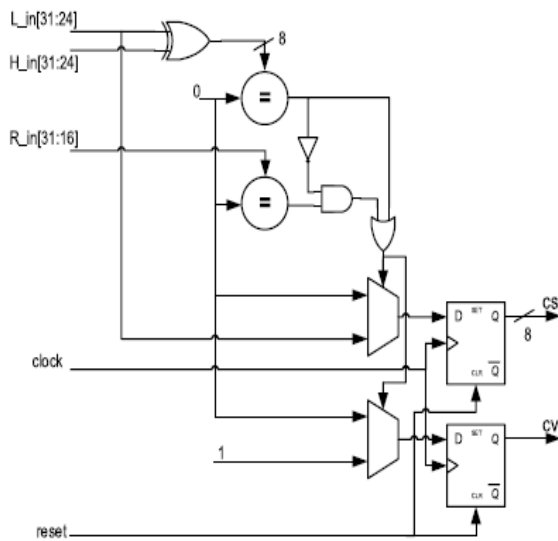

Fig.3 (e) Renormalization architecture [1].

Fig.3(f) Bit Stream output architecture[1].

IV. CONCLUSIONS

In this paper A new efficient Adaptive Binary range Coder and its Hardware architecture is proposed. In comparison with the M-coder and the MQ-coder, the proposed ABRC achieves a better compression performance in the case of image and video coding based on wavelet transform, It does not use additional memory such as lookup tables, The hardware architecture is designed such that we can implement it by using FPGA so that It consumes less power and it also increases the speed of system. Therefore, it can be more attractive and efficient for future high performance image and video compression systems. In comparison with an ABRC with a single window, the proposed system provides a faster probability adaptation at the initial encoding and decoding stage, and more accurate probability estimation for very low entropy binary sources.

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