Proceedings of
INTERNATIONAL CONFERENCE ON COMPUTING, COMMUNICATION AND ENERGY SYSTEMS (ICCCES-16)
In Association with IET, UK & Sponsored by TEQIP-II
29th-30th, Jan. 2016

Paper ID: EE25

CASCADE MULTILEVEL INVERTER WITH REDUCED NUMBER OF POWER ELECTRONIC SWITCHES

Mr. Kiran M. Nathgosavi
M.Tech. (Electrical Power System)
Rajarambapu Institute of technology
Maharashtra, India

prof. Arun R. Thorat
Dept. of Electrical Engineering
Rajarambapu Institute of technology
Maharashtra, India

Abstract—This paper aims to present a new multilevel inverter with reduced number of power electronic switches.

For the high power demand highly developed power electronics converters are necessary. So that multilevel power converters has been launched as an substitute in high power and medium voltage situations. Multilevel inverter not only gets high power rating but also advance performance of whole system in terms of harmonics and dv/dt stress.

Since as the output levels increases the requirement of power switches and sources is increases. The paper presents a new multilevel inverter which requires less power switches. So that the setting up space and cost of inverter is decreases. These features are obtaining by comparing proposed multilevel inverter with conventional cascade multilevel inverter. The performance of the developed multilevel inverter is confirmed with computer simulations using MATLAB software and laboratory prototype implementation.

Keywords—sub-multilevel unit; cascade multilevel inverter; fundamental control system; H-bridge.

I. INTRODUCTION

Now a day's multilevel concept looks to be an alternative, economical and efficient solution for medium and high power application. In-fact, for a standard voltage grid, it is difficult to connect only one power semiconductor toggle directly [1]. So that, a multilevel power converter arrangement has been recognized as an option in high power and medium voltage situation such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on. As a cost efficient solution, multilevel converter not only achieve high power ratings, but also consent to the use of low power application in renewable energy sources such as photovoltaic, wind, and fuel cells which can be easily interconnect to a multilevel converter system for a high power application.

The series connection of switching power devices has big difficulty [2], such as, non identical distribution of applied voltage across series-connected devices that outcomes the applied voltage of separate devices much higher than blocking voltage of the devices throughout transient and steady-state condition.

To answer the above-mentioned problems successfully, a number of circuit topologies of multilevel inverter and converter have been established [3],[4] such as,

diode-clamped (or neutral-clamped),

flying capacitors (or capacitor-clamped),

Cascaded H-bridge cells with separate DC sources.

The output voltage of the multilevel inverter consists of many levels produced by using several DC voltage sources. Definitely, the quality of the produced voltage is improved as the number of voltage levels increases, so the quantity of output filters can be reduces [5].

Theoretically, it is possible to produce an infinite output voltage level. By increasing the number of levels in the inverter, the output voltage levels have more steps generating a staircase waveform, which results a reduced harmonic distortion. On the other hand, a large number of levels increase the number of switches required, gate-amp, diodes, and other components. Because of this control system become more complex and brings in a voltage imbalance problems. Therefore, these multilevel inverter systems are not appropriate for raising the output voltage levels because of their large number of switches. To boost the number of the output voltage levels so as to obtain high quality output voltage waveform by means of multilevel inverter systems, the above problems should be solved in advance [6], [7], [8]

Two topologies for dc to ac conversion are presented in this paper.

A. cascade H-bridge multilevel inverter

Cascaded H-Bridge (CHB) topology as shown in fig.1. This is become very well-liked in high-power AC supplies. A cascade multilevel inverter contains a series of H-bridge (single-phase full bridge) inverter units. Each of this H-bridge unit has its own dc source; this may be a battery unit, fuel cell or solar cell. Each separate D.C. source is associated with a single-phase full-bridge inverter. The ac terminal voltages of unlike level inverters are linked in series. Throughout the different arrangements of the four switches, S1-S4, each converter level can construct three unlike voltage outputs,

Paper ID: EE25

+Vdc, -Vdc and zero. The AC outputs of different full-bridge converters are linked in series such that the created voltage waveform is the sum of the individual converter outputs.

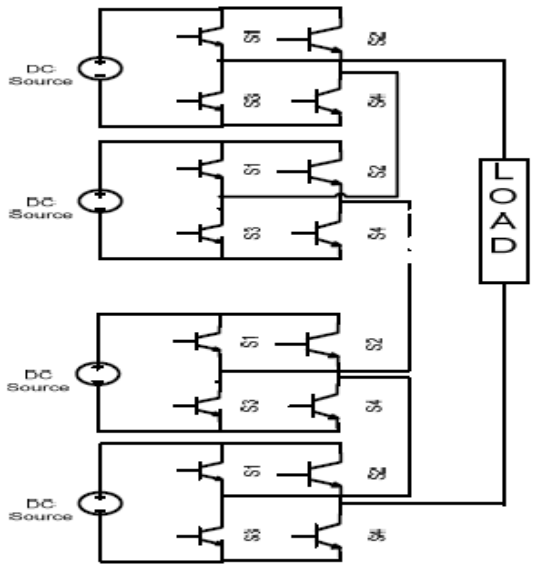


Fig.1 cascade H-bridge multilevel inverter

In this topology, the number of output voltage levels is given by

$$m = 2N+1$$

Where N is the number of DC sources.

For example a fifteen-level cascaded converter, consists of seven DC sources and seven full bridge converters. Least harmonic distortion can be achieved by controlling the conducting angles at special converter levels. Each H-bridge unit produce a quasi-square waveform by phase shifting its positive and negative phase legs switching periods. Each switching device constantly conducts for 180° (or half cycle) in spite of the pulse width of the quasi-square wave. Due to this switching method all of the switching devices current stress is equal. This new converter can avoid additional clamping diodes or voltage balancing capacitors.

The grouping of the 180° conducting method and the pattern-swapping scheme make the cascade inverters voltage and current stresses the equal and battery voltage balanced. Identical H-bridge inverter units can be developing, thus improving modularity and manufacturability and significantly reducing production costs. Electromagnetic interference (EMI) and common mode voltage are also much less as compare to PWM inverter because of the essentially low dv/dt and sinusoidal voltage output.

The main merits of using the cascade inverter [9] is,

1. Dc bus regulation is simple
2. Modified control systems can be achieved. In this each full bridge modulated separately.
3. As compare to other two topologies less number of components are used.
4. Soft switching is achieved so that switching losses are less.

   It has some demerits such as, need separate dc source for each full bridge.

B. Proposed Multilevel inverter with reduced switches

The proposed sub-multilevel unit is shown in fig.2 as shown the sub-multilevel unit consists of five switches and three dc sources. Here the switches used are unidirectional switches. To avoid the short circuit condition dc source, power switches {S2,S4},{S1,S3,S4,S5},{S1,S2,S3,S5} should not on at same time. Table-I shows the switching sequence of the proposed sub-multilevel unit.

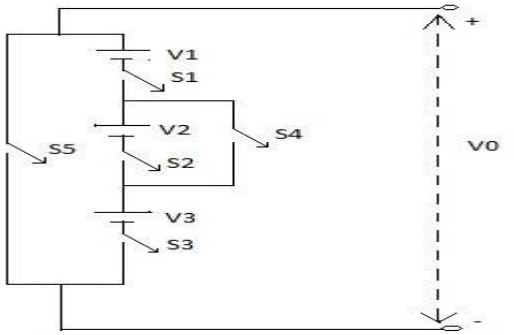


Fig.2 proposed sub-multilevel unit

It is easily understand the turn on and off state of power switches from TABLE-I. The proposed sub-multilevel unit is able to generate three dissimilar levels of 0, V1 + V3, and (V1 + V2 + V3) at the output. It is important to note that the sub-multilevel unit is no more than able to produce positive levels at the output

TABLE I
TURN ON AND OFF STATES FOR SWITCHES IN SUB-MULTILEVEL UNIT

Sr No.	Switches state					Vo
	S1	S2	S3	S4	S5	
1	Off	Off	Off	Off	On	0
2	On	Off	On	On	Off	V1+V3
3	On	On	On	Off	Off	V1+V2+V3

Paper ID: EE25

It is feasible to join n number of sub-multilevel units in series. As this inverter is able to generate all voltage levels instead of V1, it is essential to use an additional dc voltage source with the magnitude of V1 and two unidirectional switches that are added in string with the planned units. Fig. 3a shows the proposed cascaded inverter which is able to produce all levels at the output. In this inverter, to produce the least output level switches S1 and S2 and dc voltage source V1 have been used. The amplitude of minimum output voltage level is indicated by voltage source V1=Vdc. The output voltage level of each unit is represented by Vo,1, Vo,2,…,Vo,n.

The output voltage Vo of the planned cascaded multilevel inverter is equal to,

$$v_0(t) = v_{0,1}(t) + v_{0,2}(t) + \cdots + v_{0,n}(t) + v_0'(t)$$

Table-II shows switching sequence of proposed inverter. As the proposed inverter only able to generate positive voltage levels at the output it is essential to add an h-bridge. H-bridge consists of four switches T1-T4. This inverter is called the proposed cascade inverter. The load voltage will be positive that is +Vo when switch T1 and T4 are on and it is negative that is –Vo when switch T2 and T3 on.

Number of power switches and the number of dc voltage sources are given by the following equations,

$$N_{switches} = 5 * n + 6$$

$$N_{sources} = 3 * n + 1$$

n is the number of sub-multilevel units

As all switches are unidirectional switches the number of IGBTs, power diodes and driver circuits is equal to the number of power switches.

One more main parameter is to be considered while determining the total cost of the inverter. This parameter is highest amount of blocked voltage by switch. The cost of inverter is reduced as the amplitude of blocked voltage switches is reduced [10]. To determine the voltage rating of the power switch this blocked voltage value [11] plays an important role. So it is required to calculate the blocked voltage of each switch. From fig.2 value of blocked voltage by individual switch is given as,

$$V_{S1,1} = V_{S1,2} = V_{1,1}$$

$$V_{S1,j} = V_{S3,j} = \frac{V_{1,j} + V_{2,j} + V_{3,j}}{2}$$

$$V_{S4,j} = V_{S2,j} = V_{2,j}$$

$$V_{S5,j} = V_{1,j} + V_{2,j} + V_{3,j}$$

$$V_{T1} = V_{T2} = V_{T3} = V_{T4} = V_{0,max}$$

Where

Vo,max is the maximum amplitude of output voltage

the amplitude of maximum blocked voltage of proposed inverter Vblock is given by,

$$V_{block} = \sum_{j=1}^{n} V_{block,j} + V'_{block} + V_{block,H}$$

Where,

Vblock, j = blocked voltage by the jth basic unit

V_block = blocked voltage by the additional dc voltage sources

Vblock,H = blocked voltage by the used H-bridge

TABLE III
Proposed Algorithm

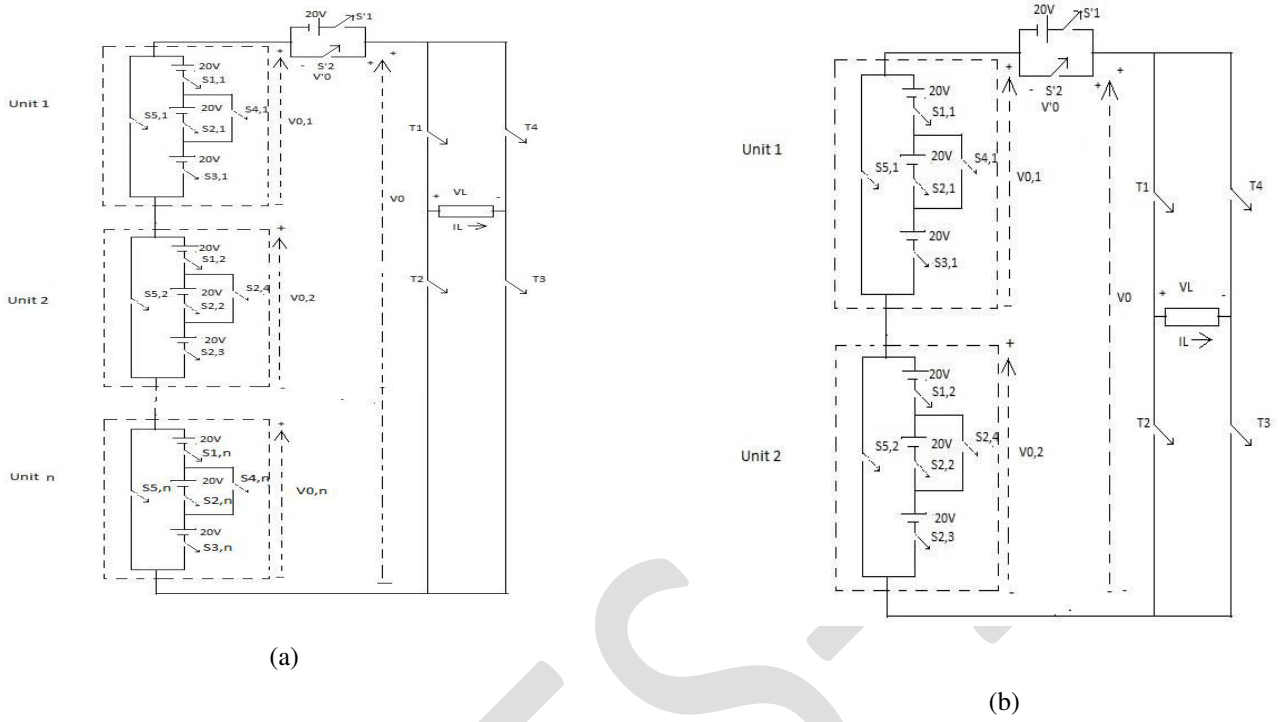
Magnitude of dc voltage source	Nlevel	Vo,max	Vblock
V1,j=V2,j=V3,j=Vdc For j=1,2,…,n	6n+3	(3n+1)Vdc	(21n+6)Vdc

In the proposed inverter, the maximum amounts of the produced output levels are depend on the used sub-multilevel units. As the proposed technology is symmetric the magnitude of voltage source is same. Table-III shows the proposed algorithm and all its parameters such as maximum amplitude produced blocked voltage etc.

II. SIMULATION AND RESULT ANALYSIS

In the proposed inverter, 2 sub-multilevel units, 1 H-bridge inverter, 7 dc sources of same amplitude Vdc are used. Output waveform of voltage has 15 levels and the current waveform is same as the ideal sinusoidal wave. Current waveform consists of phase shift as compare to voltage because of

Paper ID: EE25



(a) (b)

Fig 3 proposed topology (a) n level cascade multilevel inverter (b) 15 level multilevel inverter

TABLE II

GENERATED 15 LEVEL OUTPUT VOLTAGE BASED ON THE ON AND OFF STATE OF POWER SWITCHES

	For Positive Cycle								For Negative Cycle						
Switches	0	1	2	3	4	5	6	7	-1	-2	-3	-4	-5	-6	-7
S1a	0	1	0	0	1	0	0	1	1	0	0	1	0	0	1
S2a	0	0	1	1	0	1	1	0	0	1	1	0	1	1	0
S11	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1
S21	0	0	0	1	1	1	1	1	0	0	1	1	1	1	1
S31	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1
S41	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
S51	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0
S12	0	0	0	0	0	1	1	1	0	0	0	0	1	1	1
S22	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1
S32	0	0	0	0	0	1	1	1	0	0	0	0	1	1	1
S42	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
S52	0	1	1	1	1	0	0	0	1	1	1	1	0	0	0
T1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
T2	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
T3	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1
T4	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0

Paper ID: EE25

resistive-inductive load. The total number of switches used is 16 and 7 dc sources of same amplitude are used.

The used control method [11] for proposed inverter is the fundamental control method. This control method is selected because of its low switching frequency as compared with other control methods. Due to this switching losses are reduced. It is necessary to calculate pulse width and delay angle of each pulse. For this staircase modulation technology is used.

In output waveform for +Ve Half Cycle 14 Periods is there and in –ve half cycle 14 periods so total time period is 28.

Total pulse width is 100 so $\frac{100}{28} = 3.571$ is the time period for one level.

Phase delay means, (on time period/ total time)

$$= \frac{Ton}{Ttotal}$$

Ex.

$$1/28 * 20e^{-3}$$

Where,

$20e^{-3}$ Total time Period

The simulation of proposed multilevel inverter is done in SIMULINK/MATLAB software. The proposed model of the 15 level circuits in MATLAB is shown in Fig. 3b. The dc voltage value is 20V and the load is R=5ohm and L= 5mH. So that the peak value of output waveform is 140V. Fig 4 shows the results of 15 level inverter output voltage and load current waveform. As the dc voltage Vd is varied, the Active Power and Reactive Power flow changes but the THD remains constant because the THD depends only on the profile of the wave. If the Vd is increases P and Q will also increase but the THD remains unchanged as 8.32% as shown in TABLE V. Fig 5 shows the THD of the proposed multilevel inverter.

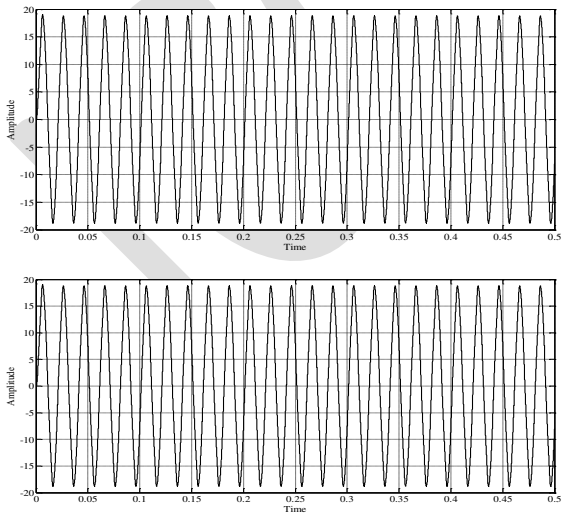


Fig. 4 15 level output voltage wave and load current

TABLE V

SIMULATION RESULT FOR PRAPOSED MULTILEVEL INVERTER

Sr.No.	Vd (Volt)	Total DC input voltage (Volt)	Active power P(W)	Reactive power Q(VAr)	THD (%)
1	5	35	50	15.67	9.04
2	10	70	200	62.65	9.04
3	15	105	450	140	9.04
4	20	140	798	250	9.04

.

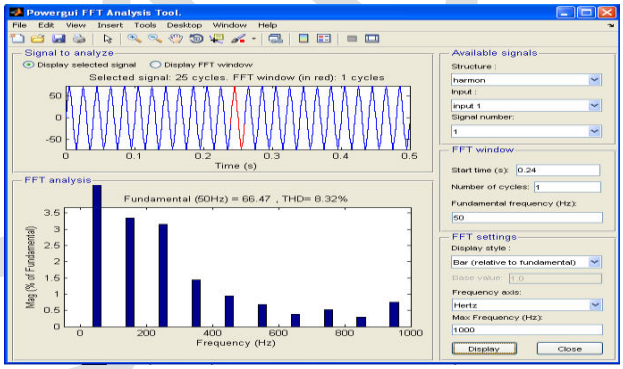


Fig.5 THD of proposed multilevel inverter

III COMPARISON

The main aim of this section is to evaluate the number of IGBTs used for a given number of voltage levels in the proposed topologies and CHB-MLI topologies. In order to have the equal situation, the proposed symmetric topology [12] is compared with the conventional symmetric CHB multilevel inverter.

As indicated in figure 6 , the planned symmetric multilevel inverter uses least number of IGBTs then the conventional MLI . For Example, for a 15-level inverter, the planned topology uses 16 IGBTs whereas the symmetric CHB multilevel inverter use 28 IGBTs.

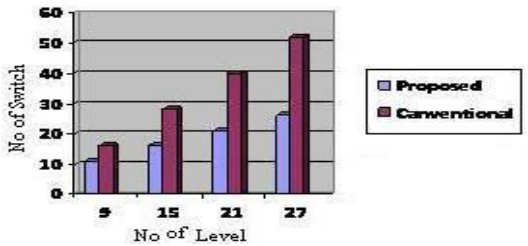


Fig 6 Variation of Nswitch versus Nlevel

Paper ID: EE25

Fig. 7 indicates the comparison of the proposed cascaded inverter with cascade H-bridge inverter on the basis of the number of driver circuits. As each switch requires a separate driver circuit, the number of driver circuits is equal to the number of power switches.

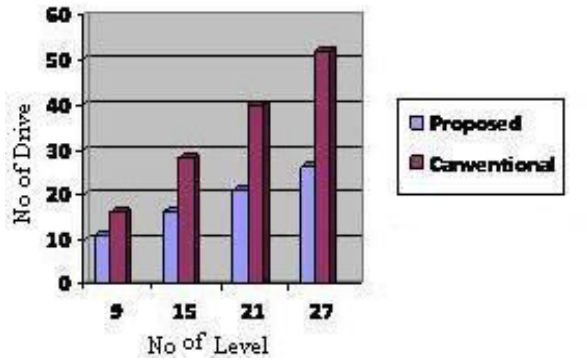


Fig 7 Variation of Ndrives versus Nlevel

As it is comprehensible from the above judgment, the developed proposed inverter has the excellent performance over conventional cascade H-bridge inverter. Reduction in the numbers of required IGBTs, power diodes, driver circuits, and dc voltage sources, and the amount of the blocked voltage by the power switches are outstanding advantages of the proposed inverter that were find out from comparisons. These advantages guide to reduction in the installation space and total cost of the inverter.

IV CONCLUSION

To eliminate the problems related with traditional CMIs, a new kind of CMI is proposed. The proposed CMI is designed with reduced power switches. The usefulness and strength of the proposed type is established with MATLAB/Simulation. Since less number of components is used, the proposed configuration is reliable, efficient, cost-effective and compact. The smart features of the proposed converters are: low switching frequency and decrease electromagnetic interference, removal of lower order harmonic component. Thus, these characteristics allow achieving good quality output voltages and inputting currents. Also it has an excellent availability due to their basic component redundancy. Due to these characteristics, proposed multilevel inverter is better than the conventional structures. The significant features of the proposed converter are well suitable for grid-connected photovoltaic/ wind-power generator, flexible alternating current systems.

REFERANCE

[1] B. P. McGrath and D. G. Holmes, "Natural capacitor voltage balancing for a flying capacitor converter induction motor drive," IEEE Trans. Power Electron. , vol. 24, no. 6, pp. 1554–1561, Jun. 2009

[2] B. Wu, High-Power Converters and AC Drives. New York: Wiley-IEEE Press, Mar. 2006

[3] A. A. Boora, A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "Voltagesharing converter to supply single-phase asymmetrical four-level diode clamped inverter with high power factor loads," IEEE Trans. Power Electron., vol. 25, no. 10, pp. 2507–2520, Oct. 2010

[4] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral point clamped inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7,pp. 2219–2230, Jul. 2010

[5] José Rodríguez, Jih-Sheng Lai, Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications" IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 49, NO. 4, AUGUST 2002

[6] E. Babaei, S. Alilu, and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge," IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3932–3939,Aug. 2014

[7] N. Farokhnia, S. H. Fathi, N. Yousefpoor, and M. K. Bakhshizadeh, "Minimizations of total harmonic distortion in a cascaded multilevel inverter by regulating of voltages DC sources," IET Power Electron., vol. 5, no. 1,pp. 106–114, Jan. 2012

[8] S. Laali, K. Abbaszadeh, and H. Lesani, "Control of asymmetric cascaded multilevel inverters based on charge balance control methods," Int. Rev. Elect. Eng., vol. 6, no. 2, pp. 522–528, Mar./Apr. 2011.

[9] E. Babaei, S. H. Hosseini, G.B. Gharehpetian, M. Tarafdar Haque and M. Sabahi, "Reduction of DC Voltage Sources and Switches in Asymmetrical Multilevel Converters Using a Novel Topology," Elsevier Journal of Electric Power Systems Research,No. 77, pp. 1073-1085, 2007

[10] Ebrahim Babaei," A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches" IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 62, NO. 2, FEBRUARY 2015

[11] E. Babaei and S. H. Hosseini, "Charge balance control methods for asymmetrical cascade multilevel converters," in Proc. ICEMS, Seoul, Korea,2007,pp.74–79

[12] M. Manjrekar and T. A. Lipo, "A hybrid multilevel inverter topology for drive application," in Proc. APEC, 1998, pp.523–529.