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ANALYSIS OF VEDIC MULTIPLIER

Akshata R.
Dept. of Electronics and Communication
Gogte Institute of Technology
Belagavi, India

Prof. V.P. Gejji
Dept. of Electronics and Communication
Gogte Institute of Technology
Belagavi, India

Prof. B.R. Pandurangi
Dept. of Electronics & Communication Engg.,
Gogte Institute of Technology
Belagavi, India

Abstract - Multipliers are extensively used in FIR filters, Microprocessors, DSP and communication applications. For higher order multiplications, a huge number of adders or compressors are to be used to perform the partial product addition. The need of low power and high speed Multiplier is increasing as the need of high speed processors are increasing. In this paper, a high performance, high throughput and area efficient architecture of a multiplier for the Field Programmable Gate Array (FPGAs) is proposed.

The most significant aspect of the proposed method is that, the developed multiplier architecture is based on vertical and crosswise structure of Ancient Indian Vedic Mathematics. As per the proposed architecture, for two 8-bit numbers; the multiplier and multiplicand, each are grouped as 4-bit numbers so that it decomposes into 4×4 multiplication modules. The coding is done in verilog and the FPGA synthesis is done using Xilinx library.

Keywords– FPGA, Multiplier, Xilinx.

I. INTRODUCTION

As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also consume considerable amount of energy. While performance and area remain to be two major design goals, power consumption has become a critical concern in today"s system design. The need of low power VLSI systems arises from two main forces. First, with the steady growth of operating frequency and processing capacity per chip, large current has to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited. Low power design directly leads to prolonged operation time in these portable devices. Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore, low power multiplier design has been an important part in low power VLSI system design. There has been extensive work on low power multipliers at technology, physical, circuit and logic levels. These low-level techniques are not unique to multiplier modules and they are generally applicable to other types of modules. The characteristics of arithmetic computation in multipliers are not considered well. Digital multipliers are the core components of all the digital signal processors (DSPs) and the speed of the DSP is largely determined by the speed of its multipliers. Two most common multiplication algorithms followed in the digital hardware are array multiplication algorithm and Booth multiplication algorithm. The computation time taken by the array multiplier is comparatively less because the partial products are calculated independently in parallel. The delay associated with the array multiplier is the time taken by the signals to propagate through the gates that form the multiplication array. Booth multiplication is another important multiplication algorithm. Large booth arrays are required for high speed multiplication and exponential operations which in turn require large partial sum and partial carry registers. Multiplication of two n-bit operands using a radix-4 booth recording multiplier requires approximately n / (2m) clock cycles to generate the least significant half of the final product, where m is the number of Booth recorder adder stages. Thus, a large propagation delay is associated with this case. Due to the importance of digital multipliers in DSP, it has always been an active area of research and a number of interesting multiplication algorithms have been reported in the literature.

In this thesis work, Nikhilam Sutra is first applied to the binary number system and is used to develop digital multiplier architecture. Urdhva tiryakbhyam Sutra is also employed and it is very similar to the popular array multiplier architecture. This Sutra also shows the effectiveness of to reduce the NXN multiplier structure into an efficient 4X4 multiplier.

II. DESCRIPTION AND ANALYSIS

VEDIC mathematics is the ancient Indian system of mathematics which mainly deals with Vedic

mathematical formulae and their application to various branches of mathematics. The word „Vedic" is derived from the word „Veda" which means the store-house of all knowledge. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krishna Tirtha (1884-1960) after his eight years of research on Vedas. According to his research, Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as Sutras. The beauty of Vedic mathematics lies in the fact that it reduces otherwise cumbersome looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. This paper discusses a possible application of Vedic mathematics to digital signal processing in the light of application of Vedic multiplication algorithm to digital multipliers. Digital multipliers are indispensable in the hardware implementation of many important functions such as fast Fourier transforms (FFTs) and multiply accumulate (MAC). This has made them the core components of all the digital signal processors (DSPs). Two most common multiplication algorithms followed in the math coprocessor are array multiplication algorithm and booth multiplication algorithm. The array multipliers take less computation time because the partial products are calculated independently in parallel. The delay associated with the array multiplier is the time taken by the signals to propagate through the gates that form the multiplication array. This paper presents a simple digital multiplier architecture based on the ancient Vedic mathematics Sutra (formula) called Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra which was traditionally used for decimal system in ancient India, this Sutra is shown to be a much more efficient multiplication algorithm as compared to the conventional counterparts. Another paper has also shown the effectiveness of this sutra to reduce the $N \times N$ multiplier structure into efficient 4×4 multiplier structures. However, they have mentioned that this 4×4 multiplier section can be implemented using any efficient multiplication algorithm. We apply this Sutra to binary systems to make it useful in such cases. In particular, we develop an efficient 4×4 digital multiplier that calculates the partial products in parallel and hence the computation time involved is less."Urdhva Tiryakbhyam" is a Sanskrit word means vertically and cross wise formula is used for smaller number multiplication. "Nikhilam Navatascaramam Dashatah" also a Sanskrit term indicating "all from 9 and last from 10", formula is used for large number multiplication. The architecture of the designed Vedic multiplier comes out to be very similar to that of the popular array multiplier and hence it should be noted that Vedic mathematics provides much simpler derivation of array multiplier than the conventional mathematics.

Urdhva Tiryakbhyam Sutra: Design and software implementation

This is the general formula which is applicable to all cases of multiplication. Urdhva Triyagbhyam means "Vertically and Crosswise", which is the method of multiplication followed.

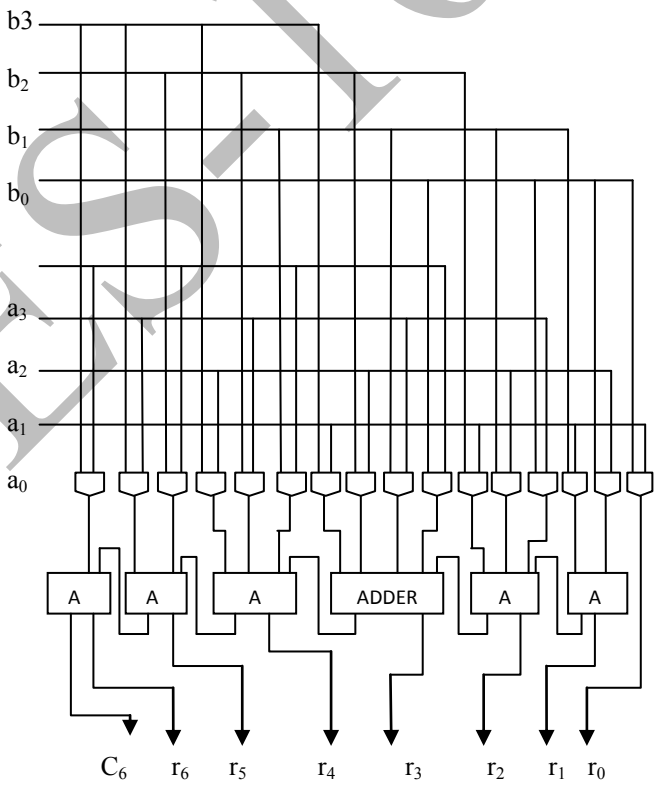

Figure 1: Hardware architecture of the Urdhva tiryakbhyam multiplier

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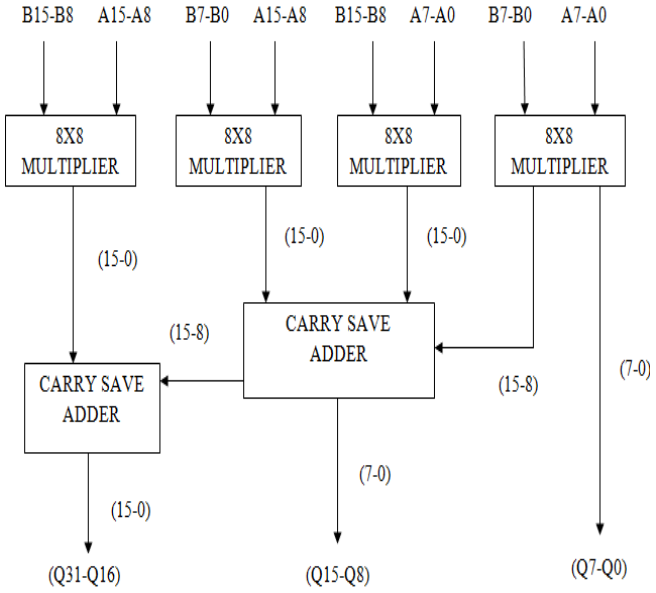

Figure 2: 16 × 16 Bits decomposed Vedic Multiplier

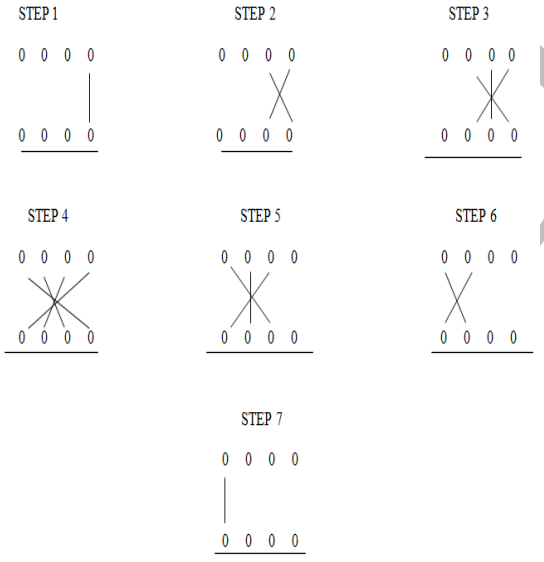

Figure 3: Line diagram

Nikhilam Sutra

Nikhilam Sutra literally means "all from 9 and last from 10". Although it is applicable to all cases of multiplication, it is more efficient when the numbers involved are large. Since it finds out the compliment of the large number from its nearest base to perform the multiplication operation on it, larger is the original number, lesser the complexity of the multiplication.

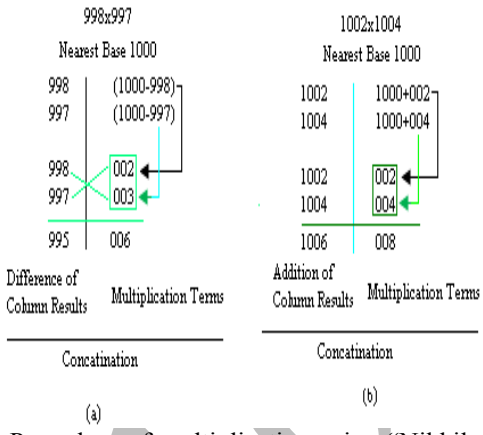

Figure 4: Procedure of multiplication using "Nikhilam Navatascharamam Dasatah" Sutra, (a) Numbers are taken below base, (b) Numbers are taken above base.

As shown in Figure 4, we write the multiplier and the multiplicand in two rows followed by the differences/addition of each of them from the chosen base. We can now write two columns of numbers, one consisting of the numbers to be multiplied (Column 1) and the other consisting of their compliments (Column 2). The product also consists of two parts which are demarcated/ incremented by a vertical line for the purpose of illustration. The right hand side (RHS) of the product can be obtained by simply multiplying the numbers of the Column 2 (2×3 = 6 or 2×4=8). The left hand side (LHS) of the product can be found by cross subtraction or addition the second number of Column 2 from the first number of Column 1 or vice versa, i.e., 998-003 = 995 or 997-002 = 995 and 1002+004=1006 or 1004+002=1006. The final result is obtained by concatenating RHS and LHS (Answer = 995006 or 1006008).

The block diagram for the implementation of the algorithm is as shown in the figure.

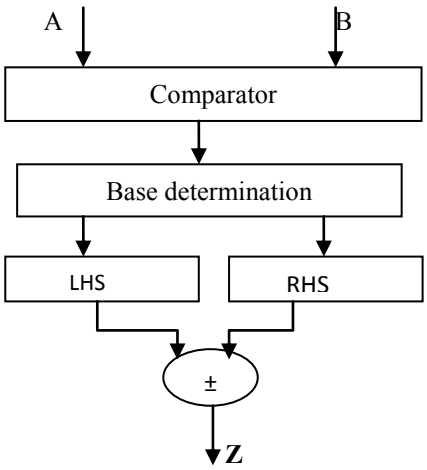

Figure 5: Block diagram of Nikhilam sutra

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Both Urdhva Thiryakbhyam and Nikhilam method are used to speed up the multiplier in this paper.

III. APPLICATIONS

1. The speed of multiplication operation is of great importance in DSP. Digital Signal processing is a technology that is present in almost every engineering discipline. It is also the fastest growing technology of the century and hence it posses tremendous challenges to the engineering community. Faster addition and multiplication are of extreme importance in DSP for Convolution, DFT and Digital filters .The core computing process is always a multiplication routine and hence DSP engineers are constantly looking for new algorithms and hardware to implement them. The methods in Vedic Multipliers are complementary directly and easy. Mr. Mangesh Karad and Mr. Chidgupkar highlight the use of multiplication process based on Vedic algorithms and implemented on 8085 and 8086 microprocessors. Use of Vedic algorithms shows appreciable saving of processing time.

2. Low power VLSI system design.

3. Frequency domain filtering (FIR and IIR), frequency-time transformations (FFT), Correlation, Digital Image processing.

4. Because of high speed of Vedic multiplication ALU utilizes this algorithm to give reliable output.

IV. RESULTS

The following figures show the simulation of Vedic Multiplier and also the RTL view of 8 and 16 bit multipliers.

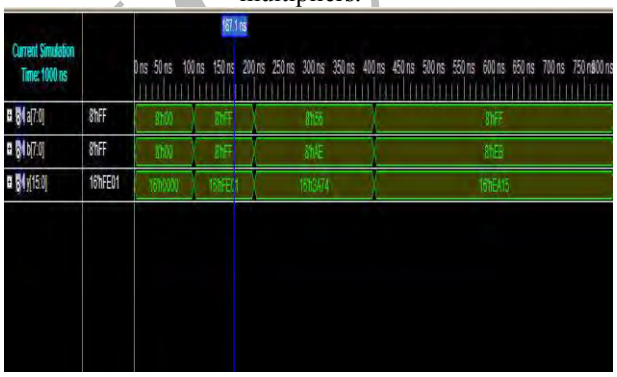

Figure 6: Simulation result of 8 × 8 bits Vedic multiplier by ISE

a : Input data 8 – bit : $FF_h = 11111111_2$
b : Input data 8 – bit : $EB_h = 11101011_2$
y : output data 16-bit: $EA15_h = 1110101000010101_2$

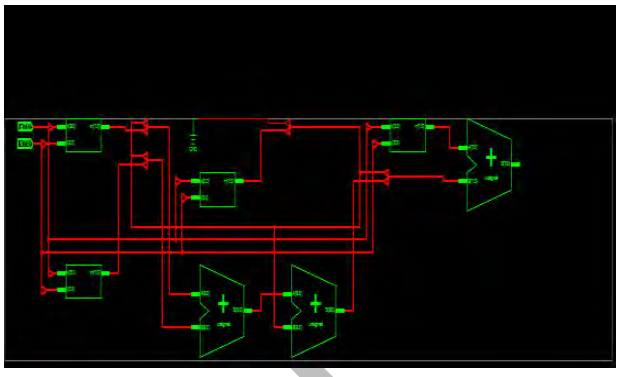

Figure 7: RTL view of 8 × 8 bits Vedic multiplier

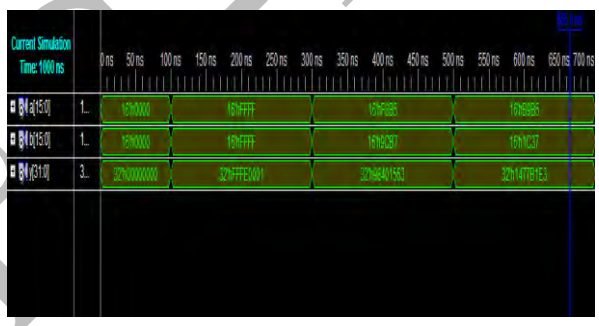

Figure 8: Simulation result of 16 × 16 bits Vedic multiplier by ISE

a : Input data 8 – bit : $FFFF_h = 1111111111111111_2$
b : Input data 8 – bit : $FFFF_h = 1111111111111111_2$
y : output data 16-bit: $FFFE0001_h = 11111111111111100000000000000001_2$

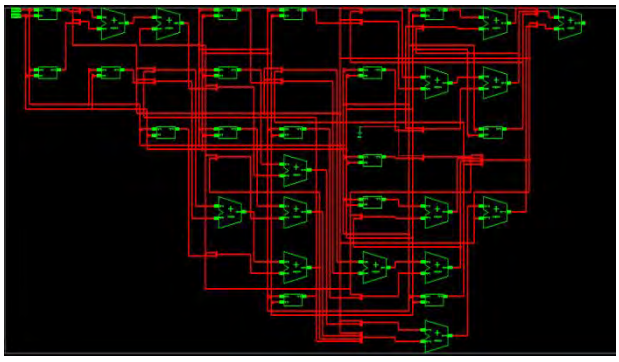

Figure 9: RTL view of 16 × 16 bits Vedic multiplier by ISE

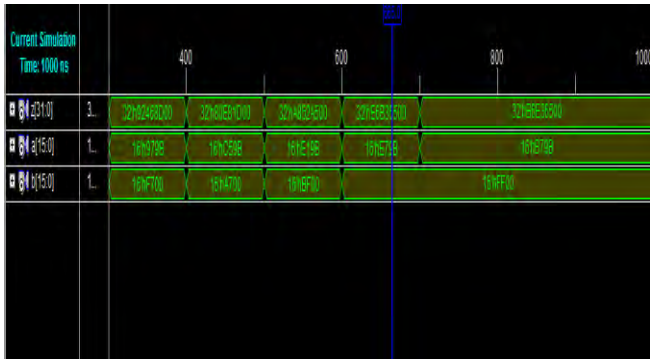

Figure 10: Simulation result of 16X16 bits Vedic multiplier(Nikhilam method) by ISE.

Figure 11: RTL view of 16X16 bits Vedic multiplier(nikhilam method)

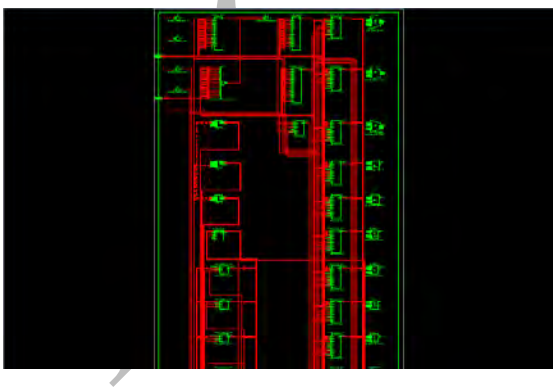

Figure 11: RTL view of 16X16 bits Vedic multiplier(nikhilam method using urdhva thirykbhyam)

From the synthesis report obtained from the Spartan 3s200 is shown in the table 1.

TABLE 1: PATH DELAY COMPARISON TABLE FOR SPARTAN 3

Sl.No.	Method	Path delay (ns)	No. of 4input LUT out of 1536	IOB out of 140	I/O'S	NO. Of slices out of 768
1.	Array 8bit	89.078	182	32	32	103
2.	Booth 8bit	36.808	237	34	34	120
3.	Vedic 8bit	23.707	133	32	32	77
4.	Array 16bit	81.989	661	64	64	378
5.	Booth 16bit	76.670	993	66	66	499
6.	Vedic 16bit	42.436	571	64	64	323
7.	Vedic Nikhilam 16 bit	36.238	1449	64	64	754
8.	Vedic using Nikhilam and Urdhva Thiryak	14.752	1330	64	64	750

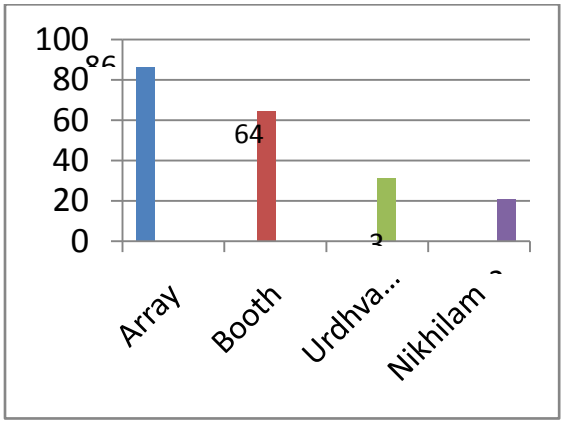

Figure.12: Time delay graph for various 16 bit multipliers

ADVANTAGES:

1. Since the partial products and their sums are calculated in parallel, the multiplier is

independent of clock frequency of processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of clock frequency.

2. Vedic multiplier has less number of gates required for given 8×8, 16×16... multipliers hence power dissipation is very small hence low power consumption i, e., power efficient.
3. As the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. The numbers of devices used in Vedic multiplier are less. Therefore it is time, space efficient.
4. The main advantage is delay increases slowly as input bits increase.
5. Vedic multiplier has greatest advantage as compared to other multipliers over gate delays and regularity of structures.
6. Highest speed among conventional multiplier.
7. It has higher throughput operations.

DISADVANTAGES:

1. Due to Urdhva tiryakbhyam structure, the system suffers from a carry propagation delay in case of large numbers.
2. As the number of bits increases above 32 or 64 bits the propagation delay in calculating RHS part of the algorithm also increases significantly.

V. FUTURE WORK

Even though Urdhva Tiryakbhyam Sutra is fast and efficient but one fact is worth noticing, that is 2×2 multiplier being the basic building block of 4×4 multiplier and so on. This leads to generation of a large number of partial products and of course, large fan out for input signals a and b. To tackle this problem, a 4×4 multiplier can be formed using other fast multiplication algorithms possible, and keeping Urdhva Tiryakbhyam for higher order multiplier blocks. Also multiplication methods like Toom Cook algorithm can be studied for generation of fewer partial products. In this work, some steps have been taken towards implementation of fast and efficient ALU or a Math Co processor, using Vedic Mathematics and maybe in near future, the idea of a very fast and efficient ALU using Vedic Mathematics algorithm is made real. Also using poorak method and subsutras of Nikhilam it is possible to implement both signed and unsigned form of multiplication with much improvement in the path delay compared to Urdhva Tiryakabhyam. As the number of bits increases above 32 or 64 bits the propagation delay in calculating RHS part of the algorithm also increases significantly. Hence to overcome this problem urdhvatiryak method can be employed at the RHS side.Vedic mathematics is long been known but has not been implemented in the DSP and ADSP processors employing large number of multiplications in calculating the various transforms like FFTs and the IFFTs. By using these ancient Indian Vedic mathematics methods world can achieve new heights of performance and quality for the cutting edge technology devices.

VI. CONCLUSION

The designs of 8×8 bits and 16×16 bits Vedic multiplier have been implemented on Spartan XC3S500-5-FG320 device. The computation delay for 16x16 bits Booth multiplier was 76.670 ns, for 16x16 bits Vedic multiplier(using Urdhva Tiryakbhyam sutra) was 42.436 ns and for 16x16 bits Vedic multiplier(using Nikhilam sutra) was 36.238 ns . It is clearly shown in the synthesis report (Table 1). It is therefore seen that the Vedic multipliers are much faster than the conventional multipliers. The algorithms of Vedic mathematics are much more efficient than of conventional mathematics.

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