DESIGN AND EVALUATION OF LVTSCR ESD PROTECTION DEVICE STRUCTURE FOR SUBMICRON CMOS LNA.

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ABSTRACT

ESD scheme of Radio Frequency integrated circuit is a large challenge as defect of the ESD device model and communication between the main LNA circuit and the protection circuit. The scaling down of technology increases the prerequisite of protection from release of inert electrical energy. The protection scheme should make less influence on the main circuit performance. In this paper, 0.13µm CMOS technology is used to design differential LNA circuit and ESD protection is implemented using Low Voltage Triggered Silicon Controlled Rectifier (LVTSCR). The Radio Frequency ESD scheme is implemented to the 4GHz to 5GHz linear zed LNA. The ESD and the RF LNA circuit scheme are proposed at its device level simulation. In this study, ESD shield is integrated by extracting S parameters. The Human Body Model of 4kV is used for the trial of main LNA circuit performance. The LNA topology used is differential LNA and enhancement in linearity is achieved by using RC feedback. The extracted results are compared as differential LNA circuit with and without ESD.

KEYWORDS-Differential LNA; CMOS; linearity; ESD protection; LVTSCR (Low-Voltage Trigger SCR).

INTRODUCTION

Electrostatic discharge guard has turn into a core concern on the trustworthiness of integrated circuit products in sub micrometer CMOS technologies. Electrostatic expulsion safety for submicron CMOS IC's is greatly ruined in line for both the reduced characterized size of down scaling of the devices and the unconventional CMOS technologies. To minimize voltage of lateral SCR device in CMOS submicron technologies; certain hard work had been added to alter the structure of lateral SCR device. An altered configuration of lateral SCR device called as LVTSCR had been conveyed with its trigger voltage lesser than that of gate-oxide breakdown voltage. By means of device sizes in progressive technologies continue to reduce integrated circuits come to be further exposed to failures from flashover. Silicon controlled rectifiers (SCRs) are regularly castoff to make available on-chip safeguard against ESD destruction for higher frequency. SCRs inhabit lesser spaces and ought to parasitic capacitance are very less than MOS ESD devices [1]-[3]. An inert energy amongst two adjacent stuffs is produced owing to charge restoring the correct balance process that encompasses a hasty release of amassed charge [7].

Electrostatic Discharge (ESD) protection is continually of a countless interest in sub-micron region in CMOS technology. The reliability in CMOS Integrated Circuits has grown into more and more severe owing to scaling down technology. Large parasitic capacitance of the device acts as short path as the frequency increases in gigahertz which greatly worsens the enactment of the central circuit owing to the incompatibility with Radio Frequency networks. An extra device is introduced due to the ESD protection structure using effects of parasites to the IC vital and extra devices as well as parasitic effects RFICs are tremendously subtle. For that reason, the ESD and its brought parasitic effects essentially are measured in Radio Frequency integrated circuit design. Concerns such in place of the parasitic capacitance, inductance, resistance, coupling noise and noise made by it can't be overlooked any longer. The centered circuit should not be affected by the addition of the ESD protection circuit. Aimed at RFIC demand tremendously extraordinary trustworthiness for wireless applications in tough surroundings but then again ESD safeguard is an emergent scheme challenge. Trials provide the justification of conventional ESD protection can extremely affect the core

circuit, even though recommended ESD protection might resolve such problem [4, 8].Nano scale CMOS technologies are necessarily used to realize RF circuits using the pluses of scaling-down characteristics size, refining high-frequency features, less ower consumption, more incorporation ability, and little charge for abundant production. The gate oxide in Nano scale CMOS technology totally cut down the electrostatic discharge (ESD) vigor of IC production. The common requisite for a marketable IC product is to permit 4-kV Human Body Model (HBM) ESD trials [5]. A progressive technology scaling aids to project little noise, high gain, and less power consumption amplifier. The linearity of CMOS is degrading by means of the scaling down the process. This has inspired a number of CMOS LNA linearization methods [6, 9, 10].

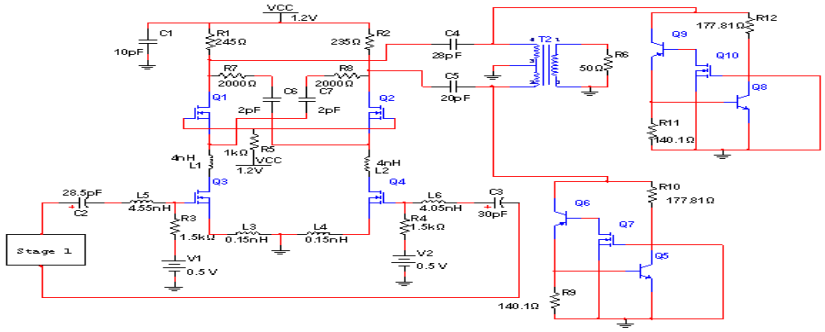


Fig. 1 LNA ESD protection with LVTSCR.

The ESD protection devices, like the diodes, BJTs, MOS, the silicon-controlled rectifier (SCR) device has been the most beneficial for RF ESD protection scheme owing to its greater ESD vigor contained by an inferior parasitic capacitance and smaller layout area. The SCR device can be used without any harm, with lacking of latch up menace in unconventional CMOS technologies using the little supply voltage [5].

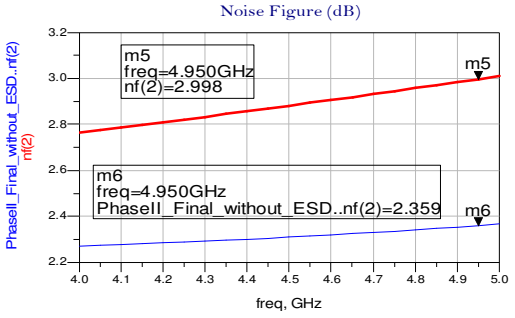
Selecting the right ESD device for a specified RF CMOS, as RF CMOS has turned into a key technology in communication systems. Radio Frequency CMOS technology for which the design of ESD protection is selected by considering points such as ESD configuration sturdiness, ESD configuration area, impedance, noise factor. RF CMOS devices that can be used for ESD protection are GGNMOS, diodes, SCR [11].

Designing the ESD protection circuit the factors that should be considered are the high stress ESD models, EDA tools which are inadequate, matching of core circuit with the protection circuit and performance based on the process technology and core circuit [4].

In this paper, we propose a differential LNA as the core RF design and ESD protection using LVTSCR. The ESD protection design is implemented for the designed LNA. Section II describes the proposed technique with the schematic diagram. Section III enlightens the experimental results, and Section IV concludes this paper.

DESIGN METHODOLOGY

Fig.1 shows the implemented LNA with ESD protection. Then ESD matching circuit is done at 4GHz-5GHz LNA. Intended for precise input impedance matching LNA is appropriately designed. Inductor at the input side provides proper impedance matching. Cascade topology is used, which advances the output impedance. Cascode topology also does the job as a reverse isolation & diminishes the change effect of output signal with respect to the input signal. The electronic device low noise amplifier intended is differential topology so that the even orders harmonics gets suppressed. Thus only the odd harmonic rapports are existent.
The first stage of LNA is designed using a noise-matching technique with inductive source degeneration. The response loop that is the feedback loop is used that overpowers the third harmonic component at the output node of the LNA. The feedback components values are 1.2KΩ and 2.0 pF for R_f and C_f. Now this, strong suit of the feedback signal is specified by value of R_f. C_f actions as a blocking DC signal and limits the central components of frequency from in flowing into feedback loop. RC response is castoff in the cross coupling form and have transfer function $T(\omega)$ between source and drain of the common gate transistor. The magnitude polarization of the transfer function $T(\omega)$, essentially remains negative, aimed at the 3rd order harmonic term at the node. It is obtained owing to the cross coupling the RC feedback



[6].

Fig. 2 Noise Figure parameter

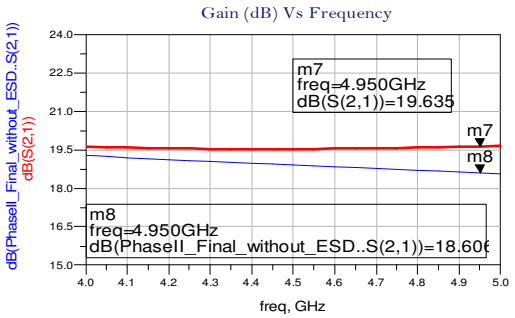


Fig. 3 Gain parameter

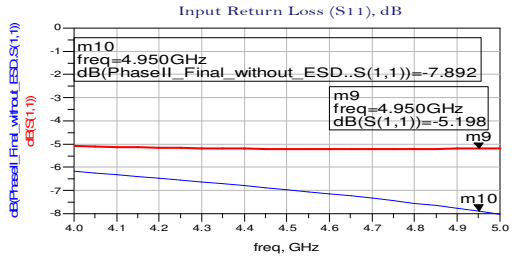


Fig. 4 Input matching

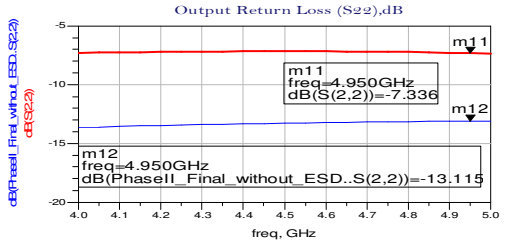


Fig. 5 Output matching

Now an RF structure, like a super heterodyne receiver, the LNA in the front-end of receiver is the first complicated structural block. LNA is regularly linked to external environment over the aerial or an off chip mast and can effortlessly be open to produce ESD. Therefore, it is evenhanded in an LNA, the ESD protection insertion in the RF chips and look after exploration with the novel technique for combining ESD circuit with core circuit [4]. In this paper, a 5 GHz Low Noise Amplifier is used using 50 Ω of impedance match at input and output side, which is employed in marketable LNA product 0.13µm CMOS process. The ESD protection circuitry used is LVTSCR.

Employing ground to the input and input to the ground are designs of 4 kV HBM model for the ESD matching networks in both directions. Meanwhile the LVTSCRs onward and inverse are identical in the dimensions, the ground to the input and input to the ground pay off curvatures of matching network of ESD illustrate related consequence. Owing to the extraordinary high act of releasing electric charge effectiveness of LVTSCR, the parasitic effects are not caused in higher level of ESD protection. Subsequently, the enactment of Radio Frequency circuit (G: gain, F: Noise Figure, stability, linearity and matching at the input and output etc.) reduces slightly [4].

Throughout the ESD incidence the shield scheme carry exact huge current for pay off and dwell in additional space of the chip. The high frequency parameters are poorly affected. For the reason that of LVTSCR completely on chip space, ESD safeguard can be efficiently implemented. Fig.1 shows the LVTSCR ESD Shield scheme with 4GHz-5GHz LNA gives the co-designed RF-ESD. SCRs must be in performance, gradually more noteworthy part in the ESD protection.

SIMULATION RESULTS

The ADS simulator is used to simulate the design. The CMOS 0.13µm process foundry PDK is used for scheme. Fig. 2 shows Noise Figure parameter of Designed LNA without and with using ESD protection. Fig. 3 shows Gain parameter, Fig. 4 and Fig. 5 shows Input matching and

TABLE I. PERFORMANCE SUMMARY

Parameters	Differential LNA Without ESD Protection	Differential LNA With ESD Protection
Frequency (GHz)	4.950	4.950
Noise Figure (dB)	2.359	2.998
Gain (dB)	18.60	19.635
Input matching (dB)	-7.892	-5.198
Output matching (dB)	-13.115	-7.336

Output matching respectively. The Table-I reviews the presentation of both electric circuit with & without ESD protection. The gain attained without ESD protection is 18.60 dB and with ESD protection is 19.63 dB, there is very small increment after use of ESD protection at frequency 4.950 GHz. The Noise Figure without ESD protection is 2.35 dB and with ESD protection is rise up to 2.99 dB, it is acceptable at the price of ESD protection. The suitable input and output matching is completed with and without ESD protection method. Table-I covers entirely the numerical values of all enactment parameter.

CONCLUSION

This paper introduces approach for designing ESD protection and Radio Frequency Integrated Circuit is concidered as the chief circuit, which includes the design of differential LNA, generating structure of ESD device LVTSCR and S-parameter extracting. These are simulated using ADS simulator. The comparisons with ESD protection scheme can be extensively used to accomplish worthy RF enactment and high ESD vigor all together. The ESD protection performance and its influence on the main LNA circuit are studied. The gain has improved slightly. ESD protection is incorporated in the RFIC at the cost of increase in Noise Figure. The comparison outcomes allow communications between ESD protection and RF core LNA circuit is also explored.

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