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THD analysis using Three and Five Level Inverter

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***Abstract*-The main disadvantage of Inverters is total harmonic distortion (THD) and harmonics. In this article, harmonics and THD are examined. A stepped multilevel inverter topology is used to suppress the harmonics generated at the inverter output. Cascading multilevel inverters are most useful for fuel cell orbattery storage power. The rated voltage of the battery is low and the cascade inverter input must be low voltage to get 230 v output. The harmonics of the single-phase load and the inverter output are investigated. Compare the harmonics and THDs of 3 and 5-level stepped multilevel inverters with conventional inverter drives. The multilevel inverter topology suppresses harmonics and THD. The result was analyzed using hardware with a spartan-3 FPGA board.**

Keywords— Inverter, Total Harmonic Distortion, cascaded multilevel inverter, 3 and 5- level MLI, Spartan-3 FPGA.

I. Introduction

Normal inverter drive or two-phase inverter drive is the most common inverter drive. Inverters have built-in harmonics that can cause the electrical power or load to heat up and shorten the life of the equipment. These concessions must be removed or eliminated and the easiest or first measure to remove the concessions is to filter the load and the inverter. filters are capacitors and inductors connected in different ways , these filters are very large and expensive. It is difficult to design and create the necessary filters. For high voltage and high power applications, multilevel (ML) inverter is a promising inverter topology and the delay introduced by these filters should be calculated . This type of inverter makes different steps of DC voltage to produce a stepped AC output that is almost a pure sine wave. Multilevel, better performance, reduced switching and switching frequency, strong power waveform, reduced dv/dt stress, low harmonics**,** low voltage measurement, etc. has advantages. Compared with 2-level inverters, the multiphase is more reliable in speed. Multilevel inverters will limit harmonics, thus reducing filter size and cost. The switching device is switched on and off in a special pattern using different DC levels to form a

multi- stage device to obtain the AC output voltage and obtain the appropriate voltage from the elimination of various relationships that would cause the AC voltage output. The amount of harmonic distortion is the smallest [1]. In this paper, a multilevel inverter topology (cascade) is used to suppress harmonics. The simulation works with 3-level and 5-level inverter topologies. The idea of H bridge inverter is connected in series to get sinusoidal output voltage. The voltage produced at the output is the sum of the voltages produced by each cell. 2n+1 output voltage levels are generated, where n represents the number of batteries. Cascading ML inverter has the advantage of using less material co mpared to terminal ML or clam-ping diode, which means the inverter is heavier than the previous two types. The number of transformers required for the n-level cascade H-bridge multilevel inverter is 2(n-1), where n represents the number of output voltage levels. Due to scarcity of fossil resources and environmental concerns, there is an increasing demand for renewable energy systems in today's world climate [2]. The most common renewable energy sources are photo-voltaic systems. The challenge is to match the output voltage and frequency to connect these systems to the grid. In photovoltaic (PV) or fuel cell (FC) applications, copper is used to lower or increase the differential and lower output voltage of the fuel cell or photovoltaic panel. The voltage and frequency req uired for the grid connection can be obtained via an inverter. Multilevel inverter can use renewable energy as it can get high power. When the multilevel inverter output voltage increases, the voltage rating of the drive does not increase. For static var generation recording, stepwise multilevel inverters hav e been proposed as renewable energy and suitable for battery use. These inverters allow renewable energy systems to be connected directly to the grid without the use of large and expensive equipment [3]. Compa red with the traditional inverter, the output voltage of the multistage inverter is stepped using the DC bus voltage, which is close to the sinusoidal voltage. The sign of a stepped output voltage suppresses the harm onic content, thereby reducing the size of the output filter. In this case, an induction motor is used as the load. Asynchronous motors consume 40% of the power and in all applications the body speed is not the measured speed. The most common control method is to use v/f, which obtains the desire d motor power by varying the frequency and voltage [12]. In this study, the simulation of the motor operat ing at 7Hz frequency was also carried out and the simulation results were obtained.

II. Multi-Level Inverter

A. Three Level Inverter

A 2-level and 3-level inverter design is nearly similar. There are two times as many regulators required in phase-leg each. The diodes are connected between upper and lower two valves. These diodes act as clamping diodes. They are connected to "n" midpoint among capacitor C1 and capacitor C2, as shown in the below figure. The "n" is neutral point. The DC-bus is built by using capacitor C1, and C2. These capacitors charged and store maximum voltage up to half i.e., Vdc/2. By using additional phase-leg, line-to-line voltage output can be obtained with additional levels. To build 0 voltages at output, the two switches are on which are closer to the midpoint and diodes (clamping) hold the voltage to 0 with respect to ground point. For getting additional voltage levels, more pairs of valve, capacitors, and diodes (clamping) are needed to be add in the design.

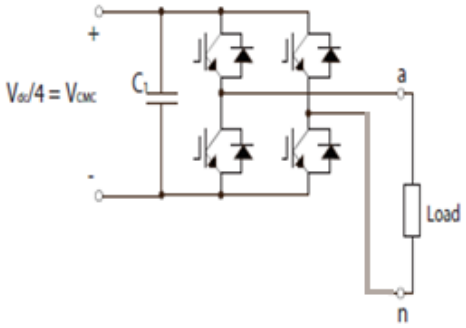

Fig. (1) 1-phase, 3-level inverter

Output Voltage	Switch state			
	S1	S2	S3	S4
0	0	0	1	1
+ Vdc/4	1	0	1	0

Table 1: States of Switches in a 3-level Cascaded Inverter.
"1" represents turned on and "0" represents turned off.

B. Five Level Inverters

In Figure (2) a base of a 5-level cascade multilevel inverter is drawn. Each Module considered as a full bridge. Hence only these modules form the CMLI topology. A full-bridge module is having at least a 3-level CMLI, and all modules cascaded to it extend the inverter to two voltage levels. In Figure 3.5b, the 2full-bridge modules produce 5 different voltage levels that can be used. Suitable applications for CMLI are, for example, where battery, photovoltaic or fuel cells are used. One example is an electric vehicle that has multiple numbers of cells (power).

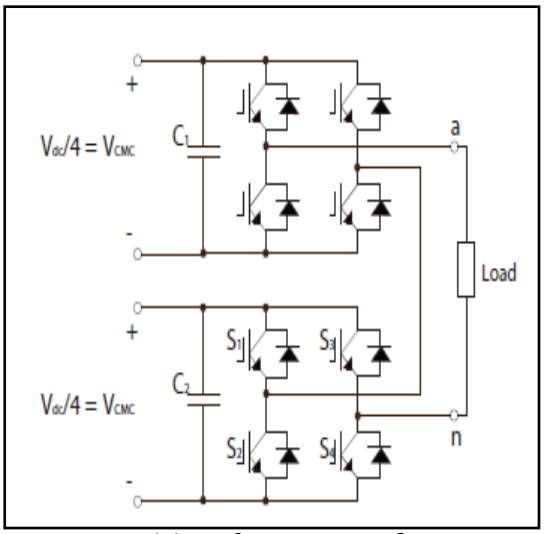

Fig. (2) 1-phase, 5-Level inverter

If adding outputs of all modules of full bridge in the inverter results in getting total voltage output and all full bridges can produce 3 voltages VCMC, 0 volt and -VCMC. CMLI turns a switch of a full-bridge module on (and off once) to change a phase output voltage level. For full-bridge modules that add VCMC voltage, switches number S1 and S4 are on, and for -VCMC, switches number S2 and S3 are turned on. 0 V if current is flowing via the full bridge. This is accomplished by turning on the 2 switches in the upper half of the full bridge (S1 and S3) or the 2 switches in the lower half (S2 and S4). Some full bridges can create stepped stepped waveforms. The maximum value of voltage output is

$$1/2\ (m-1) * VCMC = s\ VCMC = 1/2\ Vdc$$

and the minimum value of voltage is

$$1/2\ (m-1) *(-VCMC) = s\ (-VCMC) = (-1/2Vdc)$$

Where m indicates number of output levels and s indicates the number of modules of full bridge. Note that the CMLI can output total value of the voltage source in both positive and negative directions. The magnitude of the total source (voltage) is DC bus that is why the sum of the DC side voltages In Figure 2.5, it is Vdc/2, not Vdc. All connected full-bridge inverters can give the same voltage, creating the very scalable topology.

The output voltage with switch status is shown below. In this table, some output voltages are repeated and are called redundant states.

Output Voltage	Switch state							
	S1	S2	S3	S4	S1'	S2'	S3'	S4'
0	0	0	1	1	0	0	1	1
+ Vdc/4	1	0	0	1	0	0	1	1
- Vdc/4	0	1	1	0	0	0	1	1
+Vdc/2	1	0	0	1	1	0	0	1
-Vdc/2	0	1	1	0	0	1	1	0

Table 2: States of Switches in a 5-level Cascaded Inverter.
"1" represents turned on and "0" represents turned off.

III. Results

The above circuit is built using FPGA board Spartan-3 Family. This family of FPGA is mainly designed to as per needs like high-volume and applications in cost-sensitive consumer electronics. The device used here is FPGA XC3S400PQ208.

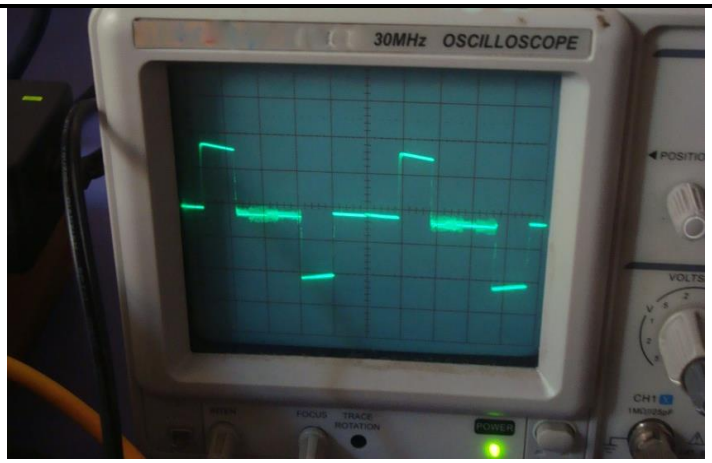

Fig. (3) output of 1-phase, 3-level inverter

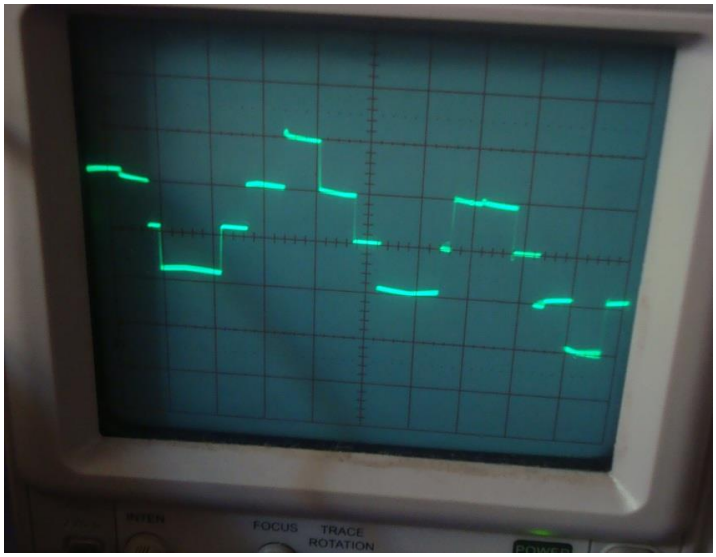

Fig. (4) output of 1-phase, 5-level inverter

Figure (3) and (4) shows output waveforms of 3 and 5 level inverters respectively. Fig. (5) and (6) shows the harmonics results of 3-level and 5-level cascaded H-bridge ML Inverter respectively.

Fig. Harmonics generated by 3-level Inverter across resistive load

Fig. Harmonics generated by 5-level Inverter across resistive load

Hence the Total Harmonic Distortion generated as

Type	% of THD
3-Level	80.10
5-Level	29.6

IV. Conclusion

The harmonic analysis and THD of 3-level and 5-level inverters using Spartan-3 hardware are examined and the results are compared with 1-phase 3 and 5-levels H-bridge multilevel inverter drivers. The results show that the harmonic can be reduced by increasing the number of levels in voltage of the inverter. From this we conclude that H-bridge stepping ML inverters are used to drive the harmonics and THD can be reduced by increasing the level.

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