Proceedings of International Conference on Sustainable Development (ICSD 2019)
In Association with Novateur Publications IJIERT-ISSN No: 2394-3696
ISBN. No. 978-93-87901-05-6
February, 14th and 15th, 2019

ICSD/80

LVDS DESIGN FOR HIGH SPEED APPLICATION

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Abstract
The devices are getting smaller due to decrease in feature size this small size makes them more area efficient as well as they operate at very high speeds, So in order to suit such a scenario while data transmission a communication protocol must be present. Low Voltage Differential Signaling (LVDS) is a used for transmission of binary data over copper cable. The main advantage of using LVDS over a normal differential pair is that LVDS consumes much less power and operates at high speed and also has a better noise immunity. This project not only designs a LVDS but also aims to provide a better speed and less power consumption as compared to its previous implementations in [2] using a lower technology and optimizing its performance for a smaller voltage level.
Keywords: CMOS, SERDES, VLSI.

1. Introduction

The technology is advancing day by day and the speed of operation is also increasing. Due to this the old parallel communication standard such as PCI and PCI-X cannot provide the required standards for high speed communication. If the parallel communication is used then it causes the skew to appear in the transmission. The inter symbol interference between the two lines will also increase as the speed of transmission is increased. Moreover due to advancement is technology the chips are getting more and more dense now if parallel communication is used in such environment the above stated phenomenon will occur and the data intended will be corrupted and will be of no use, it will require more area (as no of bits are increased the width of bus used for communication also increases in parallel communication)

Now to provide a better communication between the high speed circuits (for eg: Inter IC communication) there is a need to convert the parallel data to serial for transmission over the interface. These circuits converts the parallel data into serial data transmit it and at the receiver opposite action takes place . It has several different blocks but the main block which acts as a driver for the Serializer is LVDS(Low voltage differential Signaling). It is a high speed communication protocol which is used foe transmission of high speed data over a immune to noise environment LVDS has several different advantages over other communication protocol or even it is better than the normal differential signaling that is used for communication.

The LVDS technology helps us to transmit data more efficiently when required gigabits (GB) data rate at less power consumption. The LVDS is defined by two standards, the telecommunications industry association (TIA) defined electrical layer standard which is known as ANSI/TIA/EIA 644 and the institute for electrical and electronics engineering (IEEE) this specifies electrical characteristics of a differential and serial communication protocol. Some other high-speed differential interface technologies are LVDS, emitter coupled logic (ECL), and current mode logic (CML). But due to the use of differential signaling LVDS data transmission technique reduces electromagnetic interference (EMI)

LVDS transmits the information as difference between the voltages of two wires; these two voltages are compared at the receiver to determine whether the information send is one or zero. Transmitter here is provided with the constant current source of 3.5mA and the direction of current determines the data passing through the wire. The current passes through 100 to 120 ohms at the receiving end, this resistor is equal to the characteristics impedance of the wire which is used for transmission and then returns in the opposite direction via the other wire. This current then passes through the resistor with voltage drop of 3.5mv. Basic structure of LVDS is shown in fig-1.

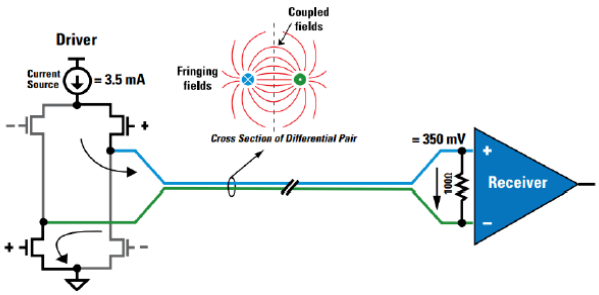

Fig-1: Low Voltage Differential Signaling [3]

LVDS reduces noise because there is tight coupling provided between the two wires. Moreover when the current passes through the two wires, the direction of flow is opposite due to which the noise or EMI developed on the wire are opposite in field and will appear as a common mode noise to the receiver. As field is opposite and coupling is tight between the wires the EMI cancels each other. Due to this the receiver is unaffected by this noise as receiver senses the difference between the two wires and voltages changes on both wires will be same

As LVDS is supplied with the constant current source the power consumption remains the same for very high operating speeds. Ground bounce effect is not present in the LVDS which is generally present in the single ended termination of the lines where the current requirements are different for transmission of one and zero

LVDS technology features include:

1. High-speed transmission capabilities up to 2 Gbps
2. Low voltage, low power consumption
3. Low noise radiation
4. Significant interference immunity due to differential signaling

LVDS has many benefits over traditional single-ended signaling topologies like parallel LVTTL/LVCMOS .The main benefits include EMI (electromagnetic interference) reduction, faster data rates, extended transmission distances, and cost/convenience.

2. Proposed LVDS Circuit.

The proposed circuit of LVDS will use a PRBS (Pseudorandom Binary Sequence) which will emitted the data sequence at high speed which will be used to transmit The Cascode Current mirror is used to provide the constant current source for the proper operation of LVDS. The driver is a differential signaling which will be based on the bits provided by PRBS.

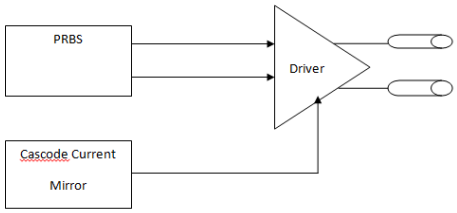

Fig-2: Proposed Diagram

2.1 PRBS (Pseudorandom Binary Sequence)

PRBS Sequence generator finds application in testing circuits such as BIST. What it basically does is generates a pattern with the help of pulse generator which is pseudo random in nature. Generally while used of specialized purpose or application such as encryption of data it is generated by certain algorithm. These computer algorithms are very complex to determine and to decrypt thus providing a good encryption for the security purposes. But the application of this PRBS here is just to emit the high speed data sequence already present in order to validate the operation of the circuit. The fig below shows a way in which a PRBS is implemented.

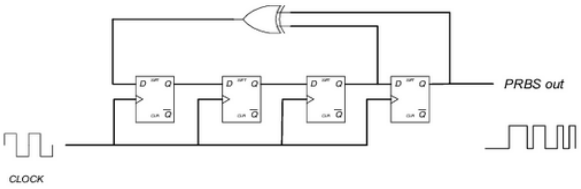

Fig-3: PRBS.

2.2 Cascode Current Mirror

The low power has different requirements than normal circuits. So in order to meet those requirements different methods have been developed. The Cascode current mirror is used to convert the supply voltage to current and then providing that constant current to the transmitter for its operation. Initially, the basic current mirrors are used for biasing purpose. The cascade current mirror has been designed to improve the O/P resistance and channel length modulation by keeping Vds8 = Vds7 Fig-4 shows the basic cascode current mirror. Due to cascade arrangement of MOS in current mirror circuit offers high gain and bandwidth. The reference current $Iref$ is defined as

$$I_{ref} = \frac{(w/l)_7(1+\lambda v_{ds7})}{(w/l)_8(1+\lambda v_{ds8})} \qquad (1)$$

w is channel width,
l is channel length and the ratio of w to l is aspect ratio of MOS,
λ is process technology parameter,
Vds is drain to source voltage.

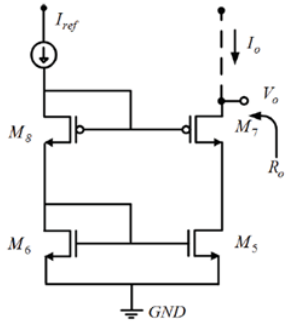

Fig-4: Cascode Current Mirror [2]

2.3 Circuit Diagram

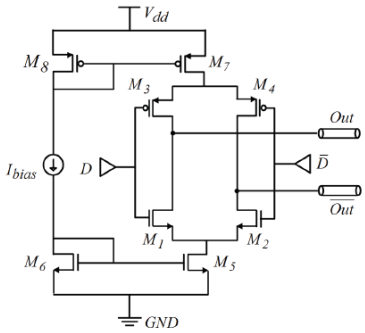

Fig-5: LVDS transmitter. [2]

The complete schematic of this LVDS transmitter has been illustrated in Fig. 5.This circuit works as current mirroring switch as well as sinking and sourcing for currents that flows to transmit the data on the transmission lines. Here, MOS M1-M4 are arranged in bridge form. If MOS M1 and M4 are OFF then M2 and M3 switches are ON and MOS M1 and M4 will be ON together when V*in*= HIGH and M2 and M3 will be ON when Vin= LOW. This transmitted data will arrive at the receiver and will be compared based on the eye diagrams. Layout will be generated for such device and will be compared with previous work stated in [2]

3. Results

The Driver circuit in Fig -5 was tested for the following and reported the following results:

DC analysis

The circuit reported similar static characteristics as inverter and also the noise margins were found to be equal which is important in order to achieve a symmetric transfer characteristic.

Transient Analysis

As transistors are matched, equal rise and fall times were reported.

PRBS source

The Driver circuit was then supplied with the input it is designed for and reported the results as shown in fig below.

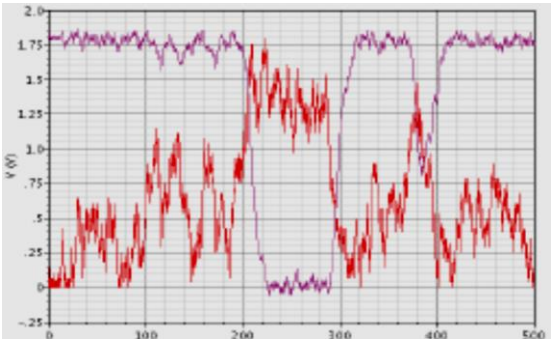

Fig-6: Eye Diagram at 2 GBPS for LVDS Driver [2]

4. Conclusion

LVDS for high speed application have been proposed which is expected to consume less power and work at higher speed than its previous implementations in [2]

Acknowledgment

We express our sincere thanks to PG Co-ordinator, Dr. M. M. Jadhav SCOE for their continues support throughout the process of this project.

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[3] https://training.ti.com/advantages-lvds.

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